

# 14 STAGE BINARY COUNTER/OSCILLATOR

**IN74HC4060A**

The IN74HC4060A is an high speed CMOS 14-STAGE BINARY COUNTER/OSCILLATOR fabricated with silicon gate C<sup>2</sup>MOS technology. The oscillator configuration allows design of either RC or crystal oscillator circuits. A high level on the CLEAR accomplishes the reset function, i.e. all counter outputs are made low and the oscillator is disabled.

A negative transition on the clock input increments the counter. Ten kinds of divided output are provided; 4 to 10 and 12 to 14 stage inclusive. The maximum division available at Q12 is 1/16384 f oscillator.

The Clock Input ( $\overline{\text{QI}}$ ) and the CLEAR input are equipped with protection circuits against static discharge and transient excess voltage.

- LOW POWER DISSIPATION:  
 $I_{CC} = 4 \mu\text{A}(\text{MAX.})$  at  $T_A = 25^\circ\text{C}$
- SYMMETRICAL OUTPUT IMPEDANCE:  
 $|I_{OH}| = I_{OL} = 4 \text{ mA}(\text{MIN})$
- BALANCED PROPAGATION DELAYS:  
 $t_{PLH} = t_{PHL}$
- WIDE OPERATING VOLTAGE RANGE:  
 $V_{CC}(\text{OPR}) = 2 \text{ V to } 6 \text{ V}$

N SUFFIX PLASTIC

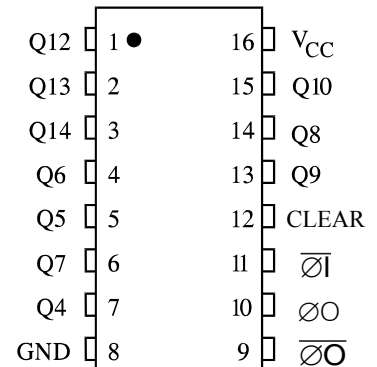
DW SUFFIX SOIC

**ORDERING INFORMATION**  
 IN74HC4060AN Plastic  
 IN74HC4060ADW SOIC  
 $T_A = -55^\circ \text{ to } 125^\circ \text{ C}$  for all packages

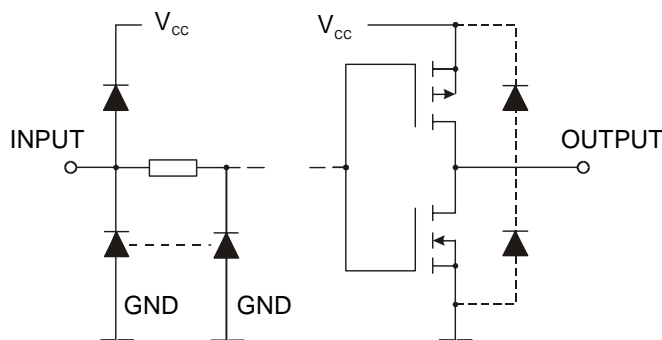
## PIN DESCRIPTION

PIN No	SYMBOL	NAME AND FUNCTION
01, 02, 03	Q12 to Q14	Counter Outputs
07, 05, 04, 06, 14, 13, 15	Q4 to Q10	Counter Outputs
09	$\overline{\text{CO}}$	External Capacitor Connection
10	$\text{RO}$	External Resistor Connection
11	$\overline{\text{QI}}$	Clock Input / Oscillator
12	CLEAR	Master Reset
08	GND	Ground (0V)
16	V <sub>CC</sub>	Positive Supply Voltage



## PIN ASSIGNMENT



## INPUT AND OUTPUT EQUIVALENT CIRCUIT

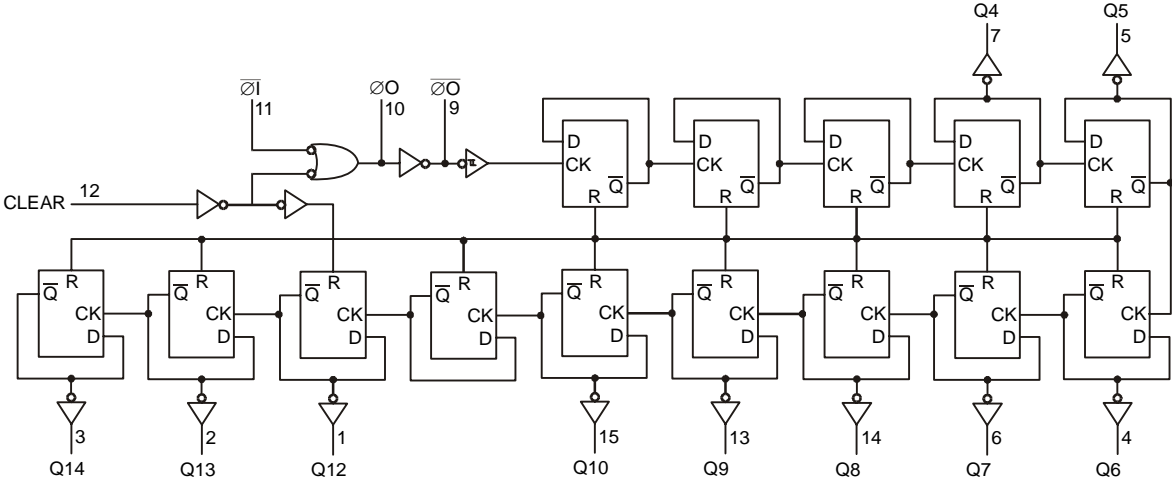


**TRUTH TABLE**

$\overline{\text{CI}}$	CLEAR	FUNCTION
X	H	COUNTER IS RESET TO ZERO STATE $\overline{\text{CO}}$ OUTPUT GOES TO HIGH LEVEL $\overline{\text{QO}}$ OUTPUT GOES TO LOW LEVEL
	L	COUNT UP ONE STEP
	L	NO CHANGE

X : Don't Care

**LOGIC DIAGRAM**



This logic diagram has not be used to estimate propagation delays

**ABSOLUTE MAXIMUM RATINGS**

Symbol	Parameter	Value	Unit
V <sub>CC</sub>	Supply Voltage	-0.5 to +7	V
V <sub>I</sub>	DC Input Voltage	-0.5 to V <sub>CC</sub> + 0.5	V
V <sub>O</sub>	DC Output Voltage	-0.5 to V <sub>CC</sub> + 0.5	V
I <sub>IK</sub>	DC Input Diode Current	± 20	mA
I <sub>OK</sub>	DC Output Diode Current	± 20	mA
I <sub>O</sub>	DC Output Current	± 25	mA
I <sub>CC</sub> or I <sub>GND</sub>	DC V <sub>CC</sub> or Ground Current	± 50	mA
T <sub>stg</sub>	Storage Temperature	-65 to +150	°C

Absolute Maximum Ratings are those values beyond which damage to the device may occur. Functional operation under these conditions is not implied

**RECOMMENDED OPERATING CONDITIONS**

Symbol	Parameter	Value	Unit	
V <sub>CC</sub>	Supply Voltage	2 to 6	V	
V <sub>I</sub>	Input Voltage	0 to V <sub>CC</sub>	V	
V <sub>O</sub>	Output Voltage	0 to V <sub>CC</sub>	V	
T <sub>OP</sub>	Operating Temperature	-55 to +125	°C	
t <sub>r</sub> , t <sub>f</sub>	Input Rise and Fall Time	V <sub>CC</sub> = 2.0 V	0 to 1000	ns
		V <sub>CC</sub> = 4.5 V	0 to 500	ns
		V <sub>CC</sub> = 6.0 V	0 to 400	ns

**DC ELECTRICAL CHARACTERISTICS**

Symbol	Parameter	Test Condition		Value				Unit
		V <sub>CC</sub> (V)		T <sub>A</sub> = 25°C		-55°C to 125°C		
				Min	Max	Min	Max	
V <sub>IH</sub>	High Level Input Voltage	2.0		1.5		1.5		V
		4.5		3.15		3.15		
		6.0		4.2		4.2		
V <sub>IL</sub>	Low Level Input Voltage	2.0			0.5		0.5	V
		4.5			1.35		1.35	
		6.0			1.8		1.8	
V <sub>OH</sub>	High Level Output Voltage (Q Output)	2.0	I <sub>O</sub> = -20 μA	1.9		1.9		V
		4.5	I <sub>O</sub> = -20 μA	4.4		4.4		
		6.0	I <sub>O</sub> = -20 μA	5.9		5.9		
		4.5	I <sub>O</sub> = -4.0 μA	4.18		4.10		
		6.0	I <sub>O</sub> = -5.2 μA	5.68		5.60		
V <sub>OL</sub>	Low Level Output Voltage (Q Output)	2.0	I <sub>O</sub> = 20 μA		0.1		0.1	V
		4.5	I <sub>O</sub> = 20 μA		0.1		0.1	
		6.0	I <sub>O</sub> = 20 μA		0.1		0.1	
		4.5	I <sub>O</sub> = 4.0 μA		0.26		0.40	
		6.0	I <sub>O</sub> = 5.2 μA		0.26		0.40	
V <sub>OH</sub>	High Level Output Voltage ( $\overline{\text{Q}}$ , $\overline{\overline{\text{Q}}}$ Output)	2.0	I <sub>O</sub> = -20 μA	1.8		1.8		V
		4.5	I <sub>O</sub> = -20 μA	4.4		4.0		
		6.0	I <sub>O</sub> = -20 μA	5.5		5.5		
V <sub>OL</sub>	Low Level Output Voltage ( $\overline{\text{Q}}$ , $\overline{\overline{\text{Q}}}$ Output)	2.0	I <sub>O</sub> = 20 μA		0.2		0.2	V
		4.5	I <sub>O</sub> = 20 μA		0.5		0.5	
		6.0	I <sub>O</sub> = 20 μA		0.5		0.5	
I <sub>I</sub>	Input Leakage Current	6.0	V <sub>I</sub> = V <sub>CC</sub> or GND		±0.1		±1	μA
I <sub>CC</sub>	Quiescent Supply Current	6.0	V <sub>I</sub> = V <sub>CC</sub> or GND		4		80	μA

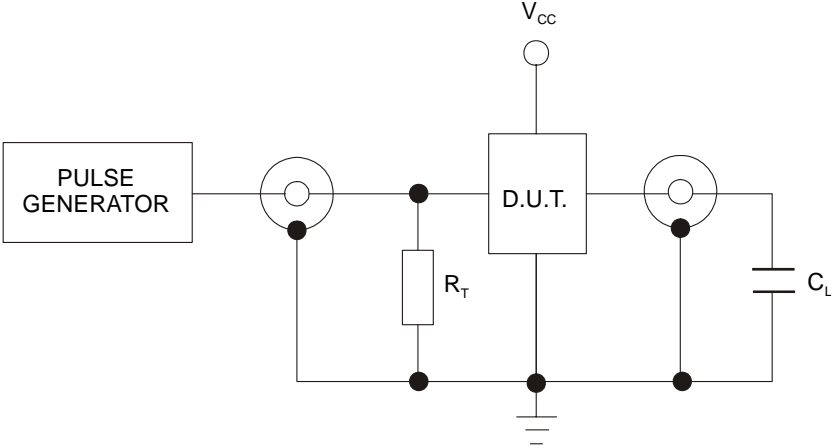
**AC ELECTRICAL CHARACTERISTICS** ( $C_L = 50$  pF, Input  $t_r = t_f = 6$  ns)

Symbol	Parameter	Test Condition		Value				Unit
		V <sub>CC</sub> (V)		T <sub>A</sub> = 25°C		-55°C to 125°C		
				Min	Max	Min	Max	
t <sub>TLH</sub> , t <sub>THL</sub>	Output Transition Time	2.0			75		110	ns
		4.5			15		22	
		6.0			13		19	
t <sub>PLH</sub> , t <sub>PHL</sub>	Propagation Delay Time ( $\overline{Q1-Q4}$ )	2.0			300		450	ns
		4.5			60		90	
		6.0			51		76	
t <sub>PD</sub>	Propagation Delay Time Difference (Q <sub>n</sub> – Q <sub>n+1</sub> )	2.0			75		110	ns
		4.5			15		22	
		6.0			13		19	
t <sub>PHL</sub>	Propagation Delay Time (CLEAR – Q <sub>n</sub> )	2.0			195		295	ns
		4.5			39		59	
		6.0			33		50	
f <sub>MAX</sub>	Maximum Clock Frequency	2.0		6		4		MHz
		4.5		30		20		
		6.0		35		24		
t <sub>W(H)</sub> , t <sub>W(L)</sub>	Minimum Pulse Width ( $\overline{Q1}$ )	2.0			75		110	ns
		4.5			15		22	
		6.0			13		19	
t <sub>W(H)</sub>	Minimum Pulse Width (CLEAR)	2.0			75		110	ns
		4.5			15		22	
		6.0			13		19	
t <sub>REM</sub>	Minimum Removal Time	2.0			100		150	ns
		4.5			20		30	
		6.0			17		26	

**CAPACITIVE CHARACTERISTICS**

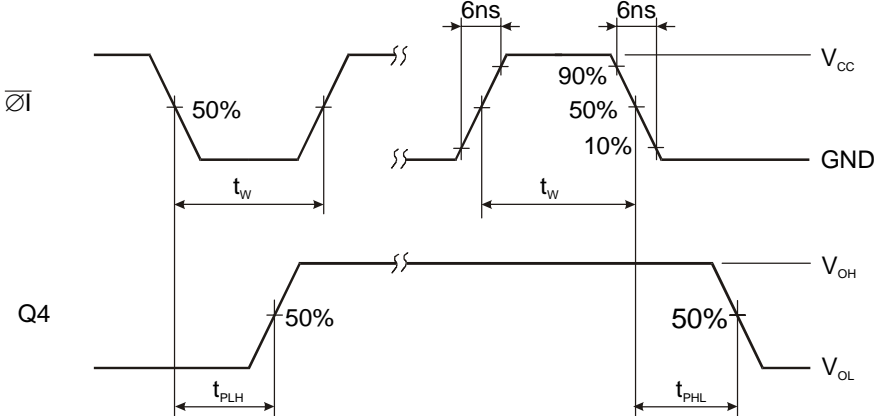
Symbol	Parameter	Test Condition		Value				Unit
		V <sub>CC</sub> (V)		T <sub>A</sub> = 25°C		-55°C to 125°C		
				Min	Max	Min	Max	
C <sub>IN</sub>	Input Capacitance	5.0			10		10	pF

**TEST CIRCUIT**

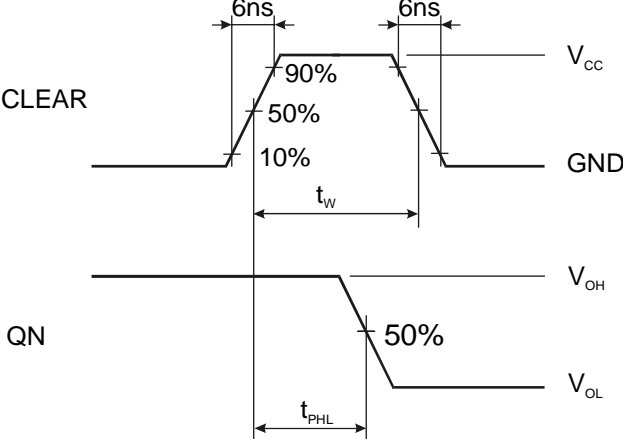


$C_L = 50 \text{ pF}$  or equivalent (includes jig and probe capacitance)  
 $R_L = Z_{OUT}$  of pulse generator (typically  $50 \Omega$ )

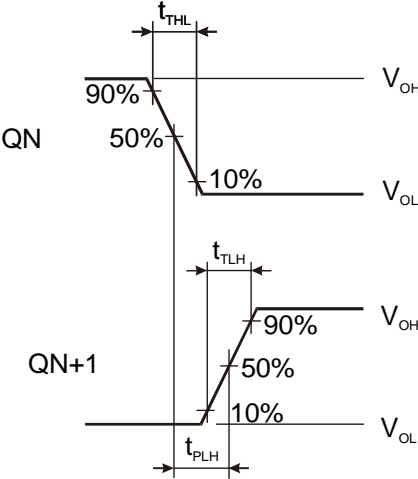
**WAVEFORM 1: PROPAGATION DELAY TIMES, MINIMUM PULSE WIDTH ( $\overline{Q1}$ ) ( $f=1\text{MHz}$ ; 50% duty cycle)**



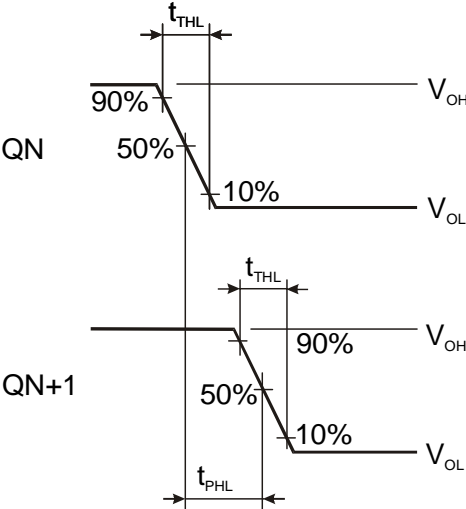
**WAVEFORM 2 : PROPAGATION DELAY TIMES, MINIMUM PULSE WIDTH (CLEAR) ( $f=1\text{MHz}$ ; 50% duty cycle)**



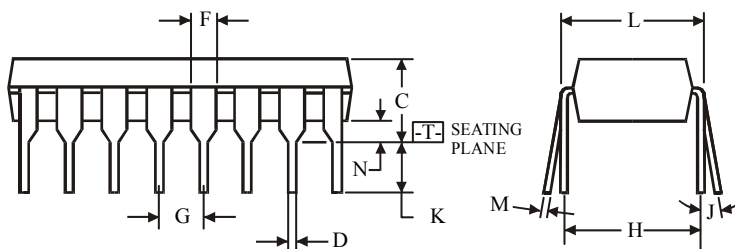
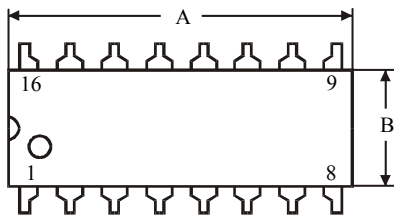
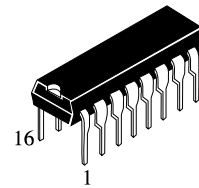
WAVEFORM 3 : PROPAGATION DELAY TIMES (f=1MHz; 50% duty cycle)



WAVEFORM 4 : PROPAGATION DELAY TIMES (f=1MHz; 50% duty cycle)



**N SUFFIX PLASTIC DIP  
(MS - 001BB)**



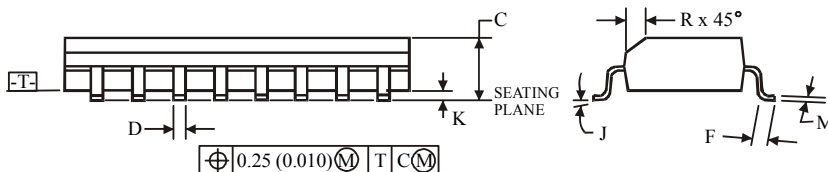
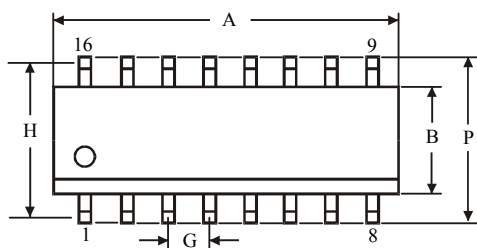
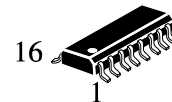
$\oplus 0.25 (0.010) \text{ (M) T}$

**NOTES:**

- Dimensions "A", "B" do not include mold flash or protrusions.  
Maximum mold flash or protrusions 0.25 mm (0.010) per side.

Symbol	Dimension, mm	
	MIN	MAX
A	18.67	19.69
B	6.1	7.11
C		5.33
D	0.36	0.56
F	1.14	1.78
G	2.54	
H	7.62	
J	0°	10°
K	2.92	3.81
L	7.62	8.26
M	0.2	0.36
N	0.38	

**D SUFFIX SOIC  
(MS - 012AC)**



$\oplus 0.25 (0.010) \text{ (M) T C (M)}$

**NOTES:**

- Dimensions A and B do not include mold flash or protrusion.
- Maximum mold flash or protrusion 0.15 mm (0.006) per side for A; for B - 0.25 mm (0.010) per side.

Symbol	Dimension, mm	
	MIN	MAX
A	9.8	10
B	3.8	4
C	1.35	1.75
D	0.33	0.51
F	0.4	1.27
G	1.27	
H	5.72	
J	0°	8°
K	0.1	0.25
M	0.19	0.25
P	5.8	6.2
R	0.25	0.5