

IN74HCT164A

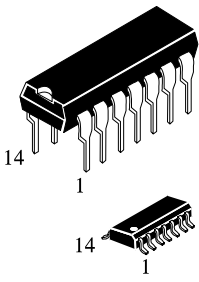
**8-BIT SERIAL-INPUT/PARALLEL-OUTPUT
SHIFT REGISTER**

High-Performance Silicon-Gate CMOS

The IN74HCT164A may be used as a level converter for interfacing TTL or NMOS outputs to high-speed CMOS inputs.

The IN74HCT164A is identical in pin out to the LS/ALS164.

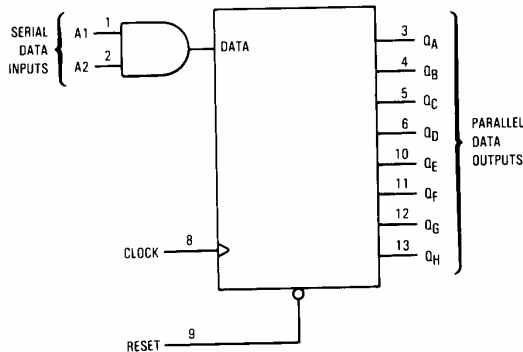
- TTL/NMOS-Compatible Input Levels.
- Outputs Directly Interface to CMOS, NMOS and TTL.
- Operating Voltage Range: 4.5 to 5.5 V
- Low Input Current: 1.0 μ A



N SUFFIX PLASTIC
D SUFFIX SOIC

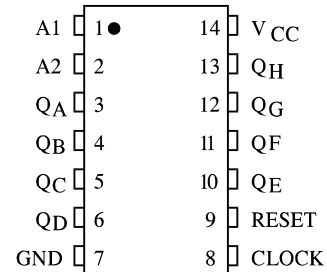
ORDERING INFORMATION
IN74HCT164AN Plastic
IN74HCT164AD SOIC
 $T_A = -55^\circ$ to 125° C for all packages

LOGIC DIAGRAM



PIN 14 = V_{CC}
PIN 7 = GND

PIN ASSIGNMENT



FUNCTION TABLE

Inputs				Outputs			
Reset	Clock	A1	A2	Q _A	Q _B	...	Q _H
L	X	X	X	L	L	...	L
H		X	X	no change			
H		H	D	D	Q _{An}	...	Q _{Gn}
H		D	H	D	Q _{An}	...	Q _{Gn}

D = data input

X = don't care

Q_{An} - Q_{Gn} = data shifted from the previous stage on a rising edge at the clock input.

MAXIMUM RATINGS*

Symbol	Parameter	Value	Unit
V _{CC}	DC Supply Voltage (Referenced to GND)	-0.5 to +7.0	V
V _{IN}	DC Input Voltage (Referenced to GND)	-1.5 to V _{CC} +1.5	V
V _{OUT}	DC Output Voltage (Referenced to GND)	-0.5 to V _{CC} +0.5	V
I _{IN}	DC Input Current, per Pin	±20	mA
I _{OUT}	DC Output Current, per Pin	±25	mA
I _{CC}	DC Supply Current, V _{CC} and GND Pins	±50	mA
P _D	Power Dissipation in Still Air, Plastic DIP+ SOIC Package+	750 500	mW
T _{stg}	Storage Temperature	-65 to +150	°C
T _L	Lead Temperature, 1 mm from Case for 10 Seconds (Plastic DIP or SOIC Package)	260	°C

*Maximum Ratings are those values beyond which damage to the device may occur. Functional operation should be restricted to the Recommended Operating Conditions.

+Derating - Plastic DIP: - 10 mW/°C from -55° to 125°C
SOIC Package: - 7 mW/°C from -55° to 125°C

RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter	Min	Max	Unit
V _{CC}	DC Supply Voltage (Referenced to GND)	4.5	5.5	V
V _{IN} , V _{OUT}	DC Input Voltage, Output Voltage (Referenced to GND)	0	V _{CC}	V
T _A	Operating Temperature, All Package Types	-55	+125	°C
t _r , t _f	Input Rise and Fall Time (Figure 1)	0	500	ns

This device contains protection circuitry to guard against damage due to high static voltages or electric fields. However, precautions must be taken to avoid applications of any voltage higher than maximum rated voltages to this high-impedance circuit. For proper operation, V_{IN} and V_{OUT} should be constrained to the range GND ≤ (V_{IN} or V_{OUT}) ≤ V_{CC}.

Unused inputs must always be tied to an appropriate logic voltage level (e.g., either GND or V_{CC}). Unused outputs must be left open.

DC ELECTRICAL CHARACTERISTICS(Voltages Referenced to GND)

Symbol	Parameter	Test Conditions	V _c V	Guaranteed Limit			Unit
				25 °C to -55°C	≤85 °C	≤125 °C	
V _{IH}	Minimum High-Level Input Voltage	V _{OUT} =0.1 V or V _{CC} -0.1 V I _{OUT} ≤ 20 μA	4.5 5.5	2.0 2.0	2.0 2.0	2.0 2.0	V
V _{IL}	Maximum Low-Level Input Voltage	V _{OUT} = V _{CC} -0.1 V I _{OUT} ≤ 20 μA	4.5 5.5	0.8 0.8	0.8 0.8	0.8 0.8	V
V _{OH}	Minimum High-Level Output Voltage	V _{IN} =V _{IH} or V _{IL} I _{OUT} ≤ 20 μA	4.5 5.5	4.4 5.4	4.4 5.4	4.4 5.4	V
		V _{IN} =V _{IH} or V _{IL} I _{OUT} ≤ 4.0 mA	4.5	3.98	3.84	3.7	
V _{OL}	Maximum Low-Level Output Voltage	V _{IN} =V _{IH} I _{OUT} ≤ 20 μA	4.5 5.5	0.1 0.1	0.1 0.1	0.1 0.1	V
		V _{IN} =V _{IH} I _{OUT} ≤ 4.0 mA	4.5	0.26	0.33	0.4	
I _{IN}	Maximum Input Leakage Current	V _{IN} =V _{CC} or GND	5.5	±0.1	±1.0	±1.0	μA
I _{CC}	Maximum Quiescent Supply Current (per Package)	V _{IN} =V _{CC} or GND I _{OUT} =0μA	5.5	1.0	10	40	μA
ΔI _{CC}	Additional Quiescent Supply Current	V _{IN} = 2.4 V, Any One Input		≥-55°C	25°C to 125°C		mA
		V _{IN} =V _{CC} or GND, Other Inputs I _{OUT} =0μA	5.5	2.9	2.4		

AC ELECTRICAL CHARACTERISTICS($V_{CC}=5.0\text{ V} \pm 10\%$, $C_L=50\text{pF}$, Input $t_r=t_f=6.0\text{ ns}$)

Symbol	Parameter	Guaranteed Limit			Unit
		25 °C to -55°C	≤85°C	≤125 °C	
f_{\max}	Maximum Clock Frequency (50% Duty Cycle) (Figures 1 and 4)	30	24	20	MHz
t_{PLH}, t_{PHL}	Maximum Propagation Delay,Clock to Q (Figures 1 and 4)	38	48	58	ns
t_{PHL}	Maximum Propagation Delay,Reset to Q (Figures 2 and 4)	41	52	63	ns
t_{TLH}, t_{THL}	Maximum Output Transition Time, Any Output (Figures 1 and 4)	15	19	22	ns
C_{IN}	Maximum Input Capacitance	10			pF
C_{PD}	Power Dissipation Capacitance (Per Package) Used to determine the no-load dynamic power consumption: $P_D=C_{PD}V_{CC}^2f+I_{CC}V_{CC}$	Typical @25°C, $V_{CC}=5.0\text{ V}$			pF
		360			

TIMING REQUIREMENTS ($C_L=50\text{pF}$,Input $t_r=t_f=6.0\text{ ns}$)

Symbol	Parameter	Guaranteed Limit			Unit
		25 °C to -55°C	≤85°C	≤125°C	
t_{SU}	Minimum Setup Time,A1 or A2 to Clock (Figure 3)	7	8	9	ns
t_h	Minimum Hold Time, Clock to A1 or A2 (Figure 3)	5	5	5	ns
t_{rec}	Minimum Recovery Time, Reset Inactive to Clock (Figure 2)	5	5	5	ns
t_w	Minimum Pulse Width, Reset (Figure 2)	12	15	20	ns
t_w	Minimum Pulse Width, Clock (Figure 1)	12	15	20	ns

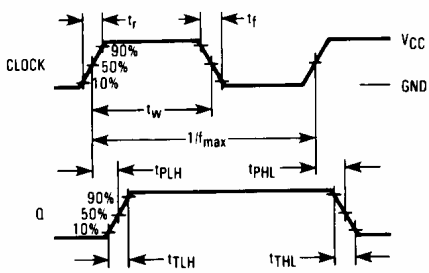


Figure 1. Switching Waveforms

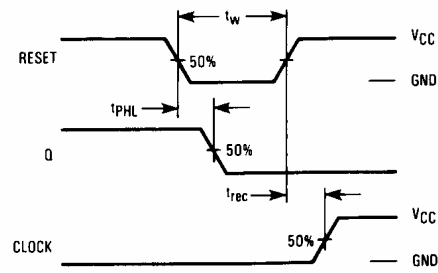


Figure 2. Switching Waveforms

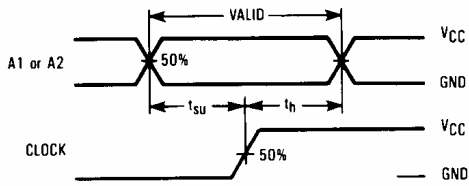
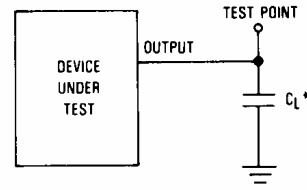


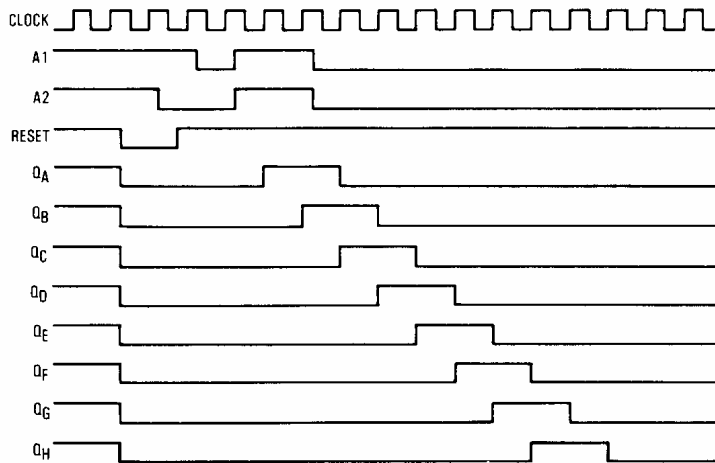
Figure 3. Switching Waveforms



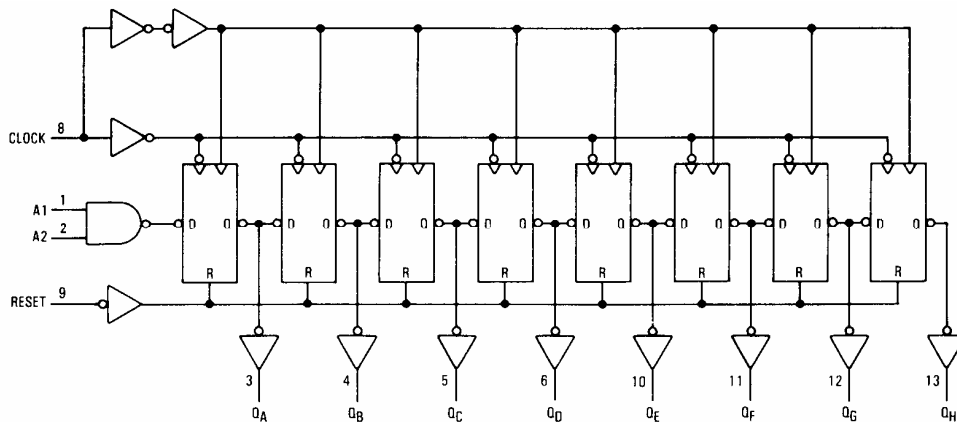
*Includes all probe and jig capacitance.

Figure 4. Test Circuit

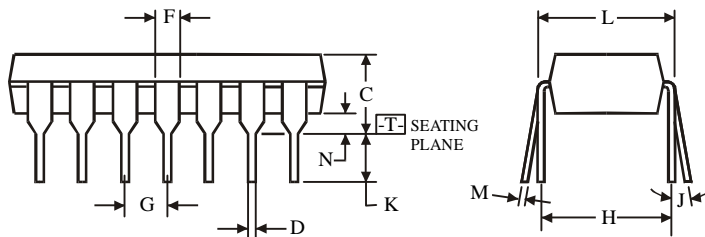
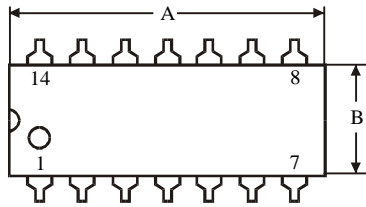
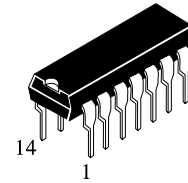
TIMING DIAGRAM



EXPANDED LOGIC DIAGRAM



N SUFFIX PLASTIC DIP
(MS - 001AA)



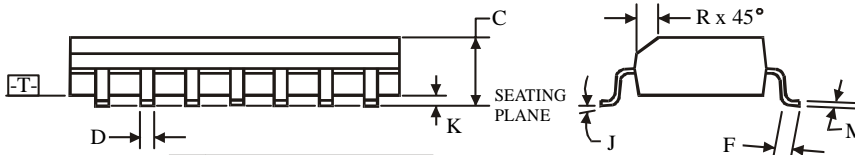
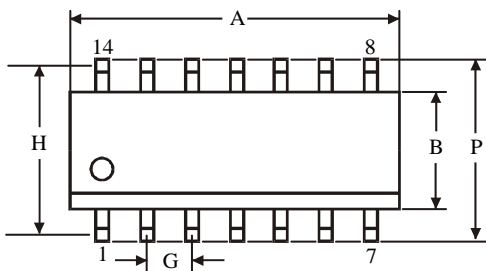
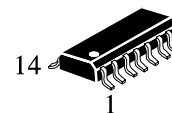
$\oplus 0.25 (0.010) \text{ (M) T}$

NOTES:

1. Dimensions "A", "B" do not include mold flash or protrusions.
Maximum mold flash or protrusions 0.25 mm (0.010) per side.

Symbol	Dimension, mm	
	MIN	MAX
A	18.67	19.69
B	6.1	7.11
C		5.33
D	0.36	0.56
F	1.14	1.78
G	2.54	
H	7.62	
J	0°	10°
K	2.92	3.81
L	7.62	8.26
M	0.2	0.36
N	0.38	

D SUFFIX SOIC
(MS - 012AB)



$\oplus 0.25 (0.010) \text{ (M) T C (M)}$

NOTES:

1. Dimensions A and B do not include mold flash or protrusion.
2. Maximum mold flash or protrusion 0.15 mm (0.006) per side for A; for B - 0.25 mm (0.010) per side.

Symbol	Dimension, mm	
	MIN	MAX
A	8.55	8.75
B	3.8	4
C	1.35	1.75
D	0.33	0.51
F	0.4	1.27
G	1.27	
H	5.27	
J	0°	8°
K	0.1	0.25
M	0.19	0.25
P	5.8	6.2
R	0.25	0.5