Low-Power Triple-Channel Digital Isolator

ILX488-3

ILX488-3 is Low-Power Triple-Channel Digital Isolator. The operating parameters of this product remain stable across wide temperature ranges throughout their service life, and only VDD bypass capacitors are required.

ILX488-3 supports with stand voltages of up to 2.5 kVRMS. This device is available in 16-pin narrow-body SOIC packages.

Features

- High-speed operation
  DC to 150Mbps
- No start-up initialization required
- Wide Operating Supply Voltage:
  2.70–5.5 V
- Ultra low power (typical)
  5 V Operation:
  < 1.6 mA per channel at 1 Mbps
  2.70 V Operation:
  < 1.4 mA per channel at 1 Mbps
- High electromagnetic immunity
- Up to 2500 VRMS isolation
- 60-year life at rated working voltage
- Precise timing (typical)
  <10 ns worst case
  1.5 ns pulse width distortion
  0.5 ns channel-channel skew
  2 ns propagation delay skew
  6 ns minimum pulse width
- Transient Immunity 25 kV/μs
- AEC-Q100 qualified
- Wide temperature range
  –40 to 125 °C at 150 Mbps
- RoHS-compliant packages
- SOIC-16 narrow body

SOIC-16 narrow

Applications

- Industrial automation systems
- Hybrid electric vehicles
- Isolated switch mode supplies
- Isolated ADC, DAC
- Motor control
- Power inverters
- Communications systems

Safety Regulatory Approvals

- UL 1577 recognized
  Up to 2500 VRMS for 1 minute
- CSA component notice 5A approval I EC 60950-1, 61010-1
  (reinforced insulation)
- VDE certification conformity
  IEC 60747-5-2
  (VDE0884 Part 2)

1. Electrical Specifications

Table 1. Recommended Operating Conditions

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Ambient Operating Temperature*	T_A	150 Mbps, 15 pF, 5 V	–40	25	125*	°C
Supply Voltage	V_{DD1}		2.70	—	5.5	V
	V_{DD2}		2.70	—	5.5	V
*Note: The maximum ambient temperature is dependent on data frequency, output loading, number of operating channels, and supply voltage.						

Table 2. Absolute Maximum Ratings[1]

Parameter	Symbol	Min	Typ	Max	Unit
Storage Temperature[2]	T_{STG}	–65	—	150	°C
Operating Temperature	T_A	–40	—	125	°C
Supply Voltage [3]	V_{DD1}, V_{DD2}	–0.5	—	6.0	V
Input Voltage	V_I	–0.5	—	V_{DD} + 0.5	V
Output Voltage	V_O	–0.5	—	V_{DD} + 0.5	V
Output Current Drive Channel	I_O	—	—	10	mA
Lead Solder Temperature (10 s)		—	—	260	°C
Maximum Isolation Voltage (1 s)		—	—	3600	V_{RMS}

Notes:
1. Permanent device damage may occur if the absolute maximum ratings are exceeded. Functional operation should be restricted to conditions as specified in the operational sections of this data sheet.
2. VDE certifies storage temperature from –40 to 150 °C.
3. See "5. Ordering Guide" on page 17 for more information.

Table 3. Electrical Characteristics

(V_{DD1} = 5 V ±10%, V_{DD2} = 5 V ±10%, T_A = –40 to 125 °C; applies to narrow SOIC packages)

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
High Level Input Voltage	V_{IH}		2.0	—	—	V
Low Level Input Voltage	V_{IL}		—	—	0.8	V
High Level Output Voltage	V_{OH}	Ioh = –4 mA	V_{DD1},V_{DD2} – 0.4	4.8	—	V
Low Level Output Voltage	V_{OL}	Iol = 4 mA	—	0.2	0.4	V
Input Leakage Current	I_L		—	—	±10	µA
Output Impedance[1]	Z_O		—	85	—	Ω
Enable Input High Current	I_{ENH}	V_{ENx} = V_{IH}	—	2.0	—	µA
Enable Input Low Current	I_{ENL}	V_{ENx} = V_{IL}	—	2.0	—	µA
DC Supply Current (All inputs 0 V or at Supply)						
V_{DD1} V_{DD2} V_{DD1} V_{DD2}		All inputs 0 DC All inputs 0 DC All inputs 1 DC All inputs 1 DC	— — — —	1.7 2.0 3.7 3.0	2.6 3.0 5.6 4.5	mA
1 Mbps Supply Current (All inputs = 500 kHz square wave, Cl = 15 pF on all outputs)						
V_{DD1} V_{DD2}			— —	2.8 2.7	4.2 4.1	mA

Timing Characteristics

Maximum Data Rate			0	—	150	Mbps
Minimum Pulse Width			—	—	6.0	ns
Propagation Delay	t_{PHL}, t_{PLH}	See Figure 2	3.0	6.0	9.5	ns
Pulse Width Distortion $\lvert t_{PLH} - t_{PHL} \rvert$	PWD	See Figure 2	—	1.5	2.5	ns
Propagation Delay Skew[2]	$t_{PSK(P-P)}$		—	2.0	3.0	ns
Channel-Channel Skew	t_{PSK}		—	0.5	1.8	ns
Output Rise Time	t_r	C_L = 15 pF See Figure 2	—	3.8	5.0	ns
Output Fall Time	t_f	C_L = 15 pF See Figure 2	—	2.8	3.7	ns
Common Mode Transient Immunity	CMTI	V_I = V_{DD} or 0 V	—	25	—	kV/µs
Enable to Data Valid[3]	t_{en1}	See Figure 1	—	5.0	8.0	ns
Enable to Data Tri-State[3]	t_{en2}	See Figure 1	—	7.0	9.2	ns
Start-up Time[3,4]	t_{SU}		—	15	40	µs

Notes:

1. The nominal output impedance of an isolator driver channel is approximately 85 Ω, ±40%, which is a combination of the value of the on-chip series termination resistor and channel resistance of the output driver FET. When driving loads where transmission line effects will be a factor, output pins should be appropriately terminated with controlled impedance PCB traces.

2. $t_{PSK(P-P)}$ is the magnitude of the difference in propagation delay times measured between different units operating at the same supply voltages, load, and ambient temperature.

3. See "3. Design Migration Guidelines" on page 13 for more details.

4. Start-up time is the time period from the application of power to valid data at the output.

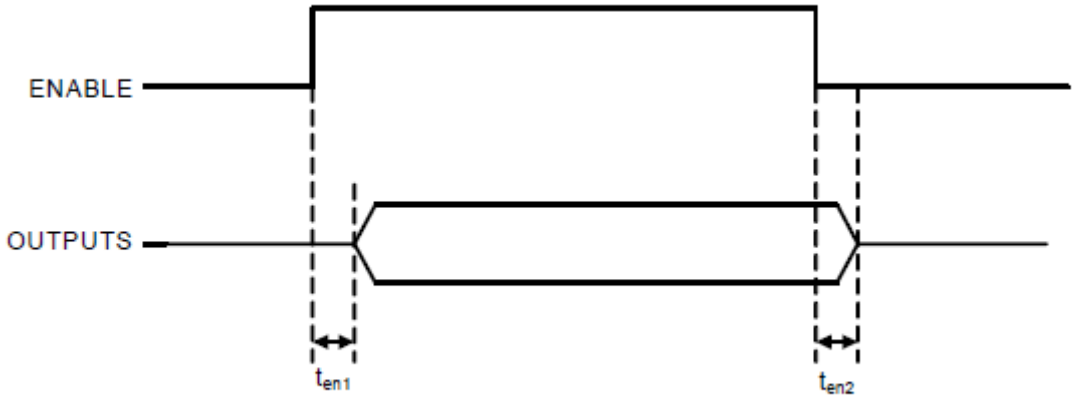


Figure 1. ENABLE Timing Diagram

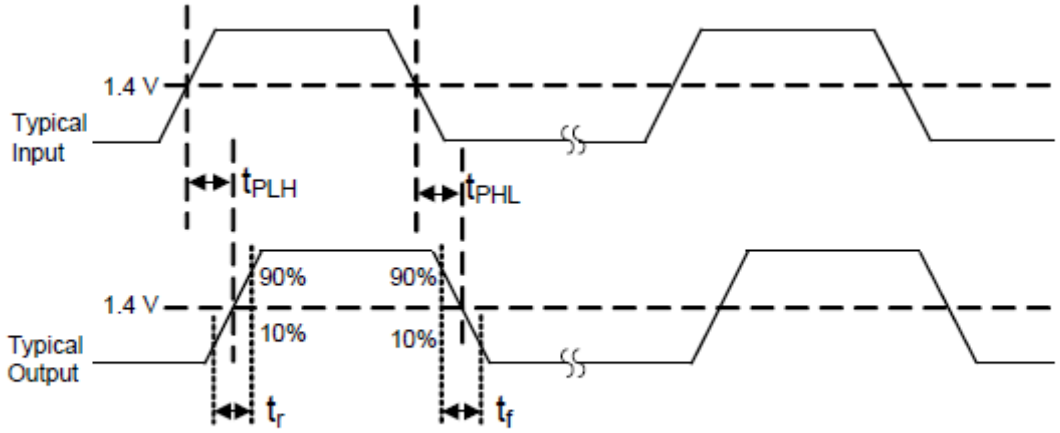


Figure 2. Propagation Delay Timing

Table 4. Electrical Characteristics

(V_{DD1} = 3.3 V ±10%, V_{DD2} = 3.3 V ±10%, T_A = –40 to 125 °C; applies to narrow -body SOIC packages)

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
High Level Input Voltage	V_{IH}		2.0	—	—	V
Low Level Input Voltage	V_{IL}		—	—	0.8	V
High Level Output Voltage	V_{OH}	Ioh = –4 mA	V_{DD1},V_{DD2} – 0.4	3.1	—	V
Low Level Output Voltage	V_{OL}	Iol = 4 mA	—	0.2	0.4	V
Input Leakage Current	I_L		—	—	±10	µA
Output Impedance[1]	Z_O		—	85	—	Ω
Enable Input High Current	I_{ENH}	$V_{ENx} = V_{IH}$	—	2.0	—	µA
Enable Input Low Current	I_{ENL}	$V_{ENx} = V_{IL}$	—	2.0	—	µA
DC Supply Current (All inputs 0 V or at supply)						
V_{DD1} V_{DD2} V_{DD1} V_{DD2}		All inputs 0 DC All inputs 0 DC All inputs 1 DC All inputs 1 DC	— — — —	1.7 2.0 3.7 3.0	2.6 3.0 5.6 4.5	mA
1 Mbps Supply Current (All inputs = 500 kHz square wave, Cl = 15 pF on all outputs)						
V_{DD1} V_{DD2}			— —	2.8 2.7	4.2 4.1	mA

Timing Characteristics

Maximum Data Rate			0	—	150	Mbps
Minimum Pulse Width			—	—	6.0	ns
Propagation Delay	t_{PHL}, t_{PLH}	See Figure 2	3.0	6.0	9.5	ns
Pulse Width Distortion $\lvert t_{PLH} - t_{PHL} \rvert$	PWD	See Figure 2	—	1.5	2.5	ns
Propagation Delay Skew[2]	$t_{PSK(P-P)}$		—	2.0	3.0	ns
Channel-Channel Skew	t_{PSK}		—	0.5	1.8	ns
Output Rise Time	t_r	C_L = 15 pF See Figure 2	—	4.3	6.1	ns
Output Fall Time	t_f	C_L = 15 pF See Figure 2	—	3.0	4.3	ns
Common Mode Transient Immunity	CMTI	$V_I = V_{DD}$ or 0 V	—	25	—	kV/µs
Enable to Data Valid[3]	t_{en1}	See Figure 1	—	5.0	8.0	ns
Enable to Data Tri-State[3]	t_{en2}	See Figure 1	—	7.0	9.2	ns
Start-up Time[3,4]	t_{SU}		—	15	40	µs

Notes:

1. The nominal output impedance of an isolator driver channel is approximately 85 Ω, ±40%, which is a combination of the value of the on-chip series termination resistor and channel resistance of the output driver FET. When driving loads where transmission line effects will be a factor, output pins should be appropriately terminated with controlled impedance PCB traces.

2. $t_{PSK(P-P)}$ is the magnitude of the difference in propagation delay times measured between different units operating at the same supply voltages, load, and ambient temperature.

3. See "3. Design Migration Guidelines" on page 13 for more details.

4. Start-up time is the time period from the application of power to valid data at the output.

Table 5. Electrical Characteristics[1]

(V_{DD1} = 2.70 V, V_{DD2} = 2.70 V, T_A = –40 to 125 ºC; applies to narrow -body SOIC packages)

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
High Level Input Voltage	V_{IH}		2.0	—	—	V
Low Level Input Voltage	V_{IL}		—	—	0.8	V
High Level Output Voltage	V_{OH}	Ioh = –4 mA	V_{DD1},V_{DD2} – 0.4	2.3	—	V
Low Level Output Voltage	V_{OL}	Iol = 4 mA	—	0.2	0.4	V
Input Leakage Current	I_L		—	—	±10	µA
Output Impedance[2]	Z_O		—	85	—	Ω
Enable Input High Current	I_{ENH}	$V_{ENx} = V_{IH}$	—	2.0	—	µA
Enable Input Low Current	I_{ENL}	$V_{ENx} = V_{IL}$	—	2.0	—	µA
DC Supply Current (All inputs 0 V or at supply)						
V_{DD1} V_{DD2} V_{DD1} V_{DD2}		All inputs 0 DC All inputs 0 DC All inputs 1 DC All inputs 1 DC	— — — —	1.7 2.0 3.7 3.0	2.6 3.0 5.6 4.5	mA
1 Mbps Supply Current (All inputs = 500 kHz square wave, Cl = 15 pF on all outputs)						
V_{DD1} V_{DD2}			— —	2.8 2.7	4.2 4.1	mA

Timing Characterisics

Maximum Data Rate			0	—	150	Mbps
Minimum Pulse Width			—	—	6.0	ns
Propagation Delay	t_{PHL}, t_{PLH}	See Figure 2	3.0	6.0	9.5	ns
Pulse Width Distortion $\lvert t_{PLH} - t_{PHL} \rvert$	PWD	See Figure 2	—	1.5	2.5	ns
Propagation Delay Skew[3]	$t_{PSK(P-P)}$		—	2.0	3.0	ns
Channel-Channel Skew	t_{PSK}		—	0.5	1.8	ns
Output Rise Time	t_r	C_L = 15 pF See Figure 2	—	4.8	6.5	ns
Output Fall Time	t_f	C_L = 15 pF See Figure 2	—	3.2	4.6	ns
Common Mode Transient Immunity	CMTI	$V_I = V_{DD}$ or 0 V	—	25	—	kV/µs
Enable to Data Valid[4]	t_{en1}	See Figure 1	—	5.0	8.0	ns
Enable to Data Tri-State[4]	t_{en2}	See Figure 1	—	7.0	9.2	ns
Start-up Time[4,5]	t_{SU}		—	15	40	µs

Notes:

1. Specifications in this table are also valid at VDD1 = 2.6 V and VDD2 = 2.6 V when the operating temperature range is constrained to T_A = 0 to 85 °C.

2. The nominal output impedance of an isolator driver channel is approximately 85Ω, ±40%, which is a combination of the value of the on-chip series termination resistor and channel resistance of the output driver FET. When driving loads where transmission line effects will be a factor, output pins should be appropriately terminated with controlled impedance PCB traces.

3. $t_{PSK(P-P)}$ is the magnitude of the difference in propagation delay times measured between different units operating at the same supply voltages, load, and ambient temperature.

4. See "3. Design Migration Guidelines" on page 13 for more details.

5. Start-up time is the time period from the application of power to valid data at the output.

Table 6. Regulatory Information*

CSA
The ILX488-3 is certified under CSA Component Acceptance Notice 5A.
61010-1: Up to 600 V_{RMS} reinforced insulation working voltage; up to 600 V_{RMS} basic insulation working voltage.
60950-1: Up to 130 V_{RMS} reinforced insulation working voltage; up to 1000 V_{RMS} basic insulation working voltage.
VDE
The ILX488-3 is certified according to IEC 60747-5-2.
60747-5-2: Up to 560 V_{peak} for basic insulation working voltage.
UL
The ILX488-3 is certified under UL1577 component recognition program.
Rated up to 2500 V_{RMS} isolation voltage for basic insulation.

***Note:** Regulatory Certifications apply to 2.5 kV_{RMS} rated devices which are production tested to 3.0 kV_{RMS} for 1 sec.

Table 7. Insulation and Safety-Related Specifications

Parameter	Symbol	Test Condition	Value	Unit
			NB SOIC-16	
Nominal Air Gap (Clearance)[1]	L(IO1)		4.9	mm
Nominal External Tracking (Creepage)[1]	L(IO2)		4.01	mm
Minimum Internal Gap (Internal Clearance)			0.008	mm
Tracking Resistance (Proof Tracking Index)	PTI	IEC60112	600	V_{RMS}
Erosion Depth	ED		0.019	mm
Resistance (Input-Output)[2]	R_{IO}		10^{12}	Ω
Capacitance (Input-Output)[2]	C_{IO}	f = 1 MHz	2.0	pF
Input Capacitance[3]	C_I		4.0	pF

Notes:
1. The values in this table correspond to the nominal creepage and clearance values as detailed in "6. Package Outline: "8. Package Outline: 16-Pin Narrow Body SOIC". VDE certifies the clearance and creepage limits as 4.7 mm minimum for the NB SOIC-16 package.
UL does not impose a clearance and creepage minimum for component level certifications. CSA certifies the clearance and creepage limits as 3.9 mm minimum for the NB SOIC-16 package.
2. To determine resistance and capacitance, the ILX488-3 is converted into a 2-terminal device. Pins 1–8 are shorted together to form the first terminal and pins 9–16 are shorted together to form the second terminal. The parameters are then measured between these two terminals.
3. Measured from input pin to ground.

Table 8. IEC 60664-1 (VDE 0844 Part 2) Ratings

Parameter	Test Conditions	Specification
Basic Isolation Group	Material Group	I
Installation Classification	Rated Mains Voltages ≤ 150 V_{RMS}	I-IV
	Rated Mains Voltages ≤ 300 V_{RMS}	I-III
	Rated Mains Voltages ≤ 400 V_{RMS}	I-II
	Rated Mains Voltages ≤ 600 V_{RMS}	I-II

Table 9. IEC 60747-5-2 Insulation Characteristics for ILX488-3*

Parameter	Symbol	Test Condition	Characteristic	Unit
Maximum Working Insulation Voltage	V_{IORM}		560	V peak
Input to Output Test Voltage	V_{PR}	Method b1 (V_{IORM} x 1.875 = V_{PR}, 100% Production Test, t_m = 1 sec, Partial Discharge < 5 pC)	1050	V peak
Transient Overvoltage	V_{IOTM}	t = 60 sec	4000	V peak
Pollution Degree (DIN VDE 0110, Table 1)			2	
Insulation Resistance at T_S, V_{IO} = 500 V	R_S		$>10^9$	Ω

***Note:** Maintenance of the safety data is ensured by protective circuits. The ILX488-3 provides a climate classification of 40/125/21.

Table 10. IEC Safety Limiting Values1

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
					NB SOIC-16	
Case Temperature	T_S		—	—	150	°C
Safety input, output, or supply current	I_S	θ_{JA} = 100 °C/W (WB SOIC-16), 105 °C/W (NB SOIC-16), V_I = 5.5 V, T_J = 150 °C, T_A = 25 °C	—	—	210	mA
Device Power Dissipation[2]	P_D		—	—	275	mW

Notes:
1. Maximum value allowed in the event of a failure; also see the thermal derating curve in Figures 3.
2. The ILX488-3 is tested with VDD1 = VDD2 = 5.5 V, TJ = 150 ºC, CL = 15 pF, input a 150 Mbps 50% duty cycle square wave.

Table 11. Thermal Characteristics

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
				NB SOIC-16		
IC Junction-to-Air Thermal Resistance	θ_{JA}		—	105	—	°C/W

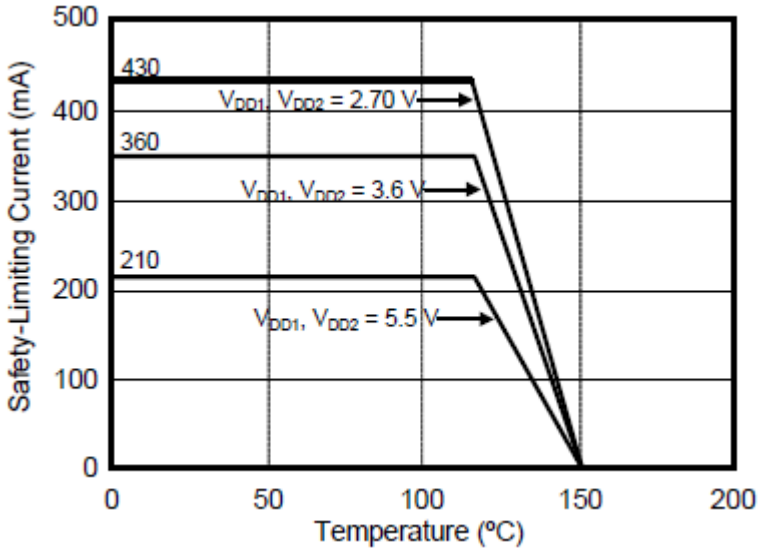


Figure 3. (NB SOIC-16) Thermal Derating Curve, Dependence of Safety Limiting Values with Case Temperature per DIN EN 60747-5-2

2. Functional Description

2.1. Theory of Operation

The operation of an ILX488-3 channel is analogous to that of an opto coupler, except an RF carrier is modulated instead of light. This simple architecture provides a robust isolated data path and requires no special considerations or initialization at start-up. A simplified block diagram for a single ILX488-3 channel is shown in Figure 4.

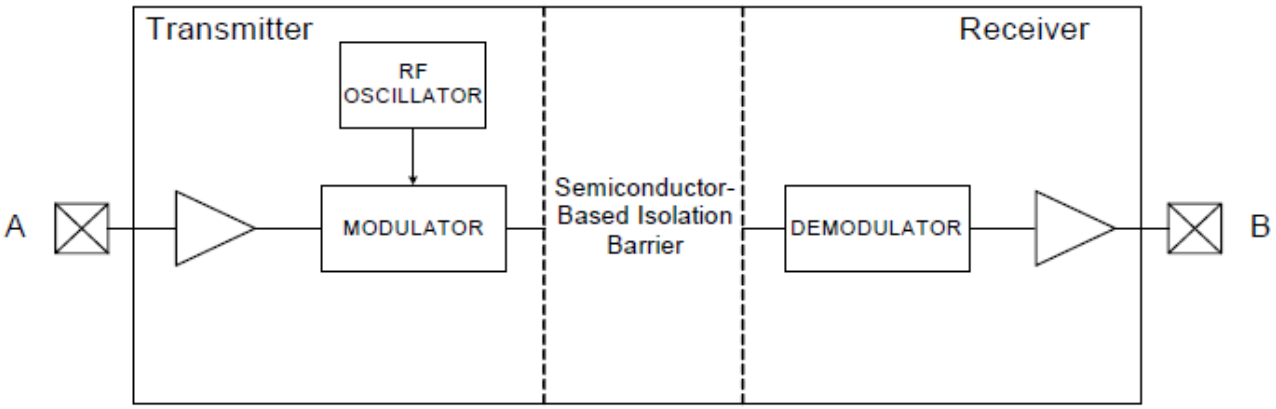


Figure 4. Simplified Channel Diagram

A channel consists of an RF Transmitter and RF Receiver separated by a semiconductor-based isolation barrier. Referring to the Transmitter, input A modulates the carrier provided by an RF oscillator using on/off keying. The Receiver contains a demodulator that decodes the input state according to its RF energy content and applies the result to output B via the output driver. This RF on/off keying scheme is superior to pulse code schemes as it provides best-in-class noise immunity, low power consumption, and better immunity to magnetic fields. See Figure 5 for more details.

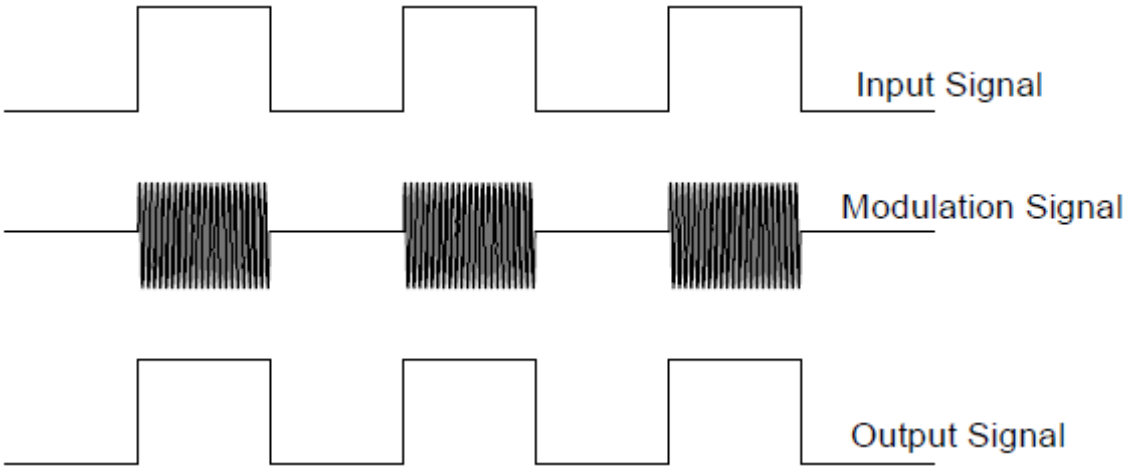


Figure 5. Modulation Scheme

2.2. Device Operation

Device behavior during start-up, normal operation, and shutdown is shown in Table 12. Table 13 provides an overview of the output states when the Enable pins are active.

Table 12. ILX488-3 Logic Operation Table

V_I Input[1,2]	EN Input[1,2,3,4]	VDDI State[1,5,6]	VDDO State[1,5,6]	V_O Output[1,2]	Comments
H	H or NC	P	P	H	Enabled, normal operation.
L	H or NC	P	P	L	
X[7]	L	P	P	Hi-Z or L[8]	Disabled.
X[7]	H or NC	UP	P	L	Upon transition of VDDI from unpowered to powered, V_O returns to the same state as V_I in less than 1 µs.
X[7]	L	UP	P	Hi-Z or L[8]	Disabled.
X[7]	X[7]	P	UP	Undetermined	Upon transition of VDDO from unpowered to powered, V_O returns to the same state as V_I within 1 µs, if EN is in either the H or NC state. Upon transition of VDDO from unpowered to powered, V_O returns to Hi-Z with 1 µs if EN is L.

Notes:
1. VDDI and VDDO are the input and output power supplies. V_I and V_O are the respective input and output terminals. EN is the enable control input located on the same output side.
2. X = not applicable; H = Logic High; L = Logic Low; Hi-Z = High Impedance.
3. It is recommended that the enable inputs be connected to an external logic high or low level when the ILX488-3 is operating in noisy environments.
4. No Connects are not internally connected and can be left floating, tied to VDD, or tied to GND.
5. "Powered" state (P) is defined as 2.70 V < VDD < 5.5 V.
6. "Unpowered" state (UP) is defined as VDD = 0 V.
7. Note that an I/O can power the die for a given side through an internal diode if its source has adequate current.
8. When using the enable pin (EN) function, outputs go into a high-impedance state when the EN pin is disabled (EN = 0). See "3. Design Migration Guidelines" on page 25 for more details.

Table 13. Enable Input Truth Table1

P/N	EN1[1,2]	EN2[1,2]	Operation
ILX488-3	H	X	Output A3 enabled and follows input state.
	L	X	Output A3 disabled and Logic Low or in high impedance state.[3]
	X	H	Outputs B1, B2 are enabled and follow input state.
	X	L	Outputs B1, B2 are disabled and Logic Low or in high impedance state.[3]

Notes:
1. Enable inputs EN1 and EN2 can be used for multiplexing, for clock sync, or other output control. These inputs are internally pulled-up to local VDD by a 3 µA current source allowing them to be connected to an external logic level (high or low) or left floating. To minimize noise coupling, do not connect circuit traces to EN1 or EN2 if they are left floating. If EN1, EN2 are unused, it is recommended they be connected to an external logic level, especially if the ILX488-3 is operating in a noisy environment.
2. X = not applicable; H = Logic High; L = Logic Low.
3. When using the enable pin (EN) function, outputs go into a high-impedance state when the EN pin is disabled (EN = 0). See "3. Design Migration Guidelines" on page 25 for more details.

2.3. Layout Recommendations

To ensure safety in the end user application, high voltage circuits (i.e., circuits with >30 VAC) must be physically separated from the safety extra-low voltage circuits (SELV is a circuit with <30 VAC) by a certain distance (creepage/clearance). If a component, such as a digital isolator, straddles this isolation barrier, it must meet those creepage/clearance requirements and also provide a sufficiently large high-voltage breakdown protection rating (commonly referred to as working voltage protection). Table 6 on page 6 and Table 7 on page 6 detail the working voltage and creepage/clearance capabilities of the ILX488-3. These tables also detail the component standards (UL1577, IEC60747, CSA 5A), which are readily accepted by certification bodies to provide proof for end-system specifications requirements. Refer to the end-system specification (61010-1, 60950-1, etc.) requirements before starting any design that uses a digital isolator.

The following sections detail the recommended bypass and decoupling components necessary to ensure robust overall performance and reliability for systems using the ILX488-3 digital isolators.

2.3.1. Supply Bypass

Digital integrated circuit components typically require 0.1 µF (100 nF) bypass capacitors when used in electrically quiet environments. However, digital isolators are commonly used in hazardous environments with excessively noisy power supplies. To counteract these harsh conditions, it is recommended that an additional 1 µF bypass capacitor be added between VDD and GND on both sides of the package. The capacitors should be placed as close as possible to the package to minimize stray inductance. If the system is excessively noisy, it is recommended that the designer add 50 to 100 resistors in series with the VDD supply voltage source and 50 to 300 resistors in series with the digital inputs/outputs (see Figure 8). For more details, see "3. Design Migration Guidelines" on page 25.

All components upstream or downstream of the isolator should be properly decoupled as well. If these components are not properly decoupled, their supply noise can couple to the isolator inputs and outputs, potentially causing damage if spikes exceed the maximum ratings of the isolator (6 V). In this case, the 50 to 300 resistors protect the isolator's inputs/outputs (note that permanent device damage may occur if the absolute maximum ratings are exceeded). Functional operation should be restricted to the conditions specified in Table 1, “Recommended Operating Conditions,” on page 2.

2.3.2. Pin Connections

No connect pins are not internally connected. They can be left floating, tied to VDD, or tied to GND.

2.3.3. Output Pin Termination

The nominal output impedance of an isolator driver channel is approximately 85Ω, ±40%, which is a combination of the value of the on-chip series termination resistor and channel resistance of the output driver FET. When driving loads where transmission line effects will be a factor, output pins should be appropriately terminated with controlled impedance PCB traces. The series termination resistor values should be scaled appropriately while keeping in mind the recommendations described in “2.3.1. Supply Bypass” above.

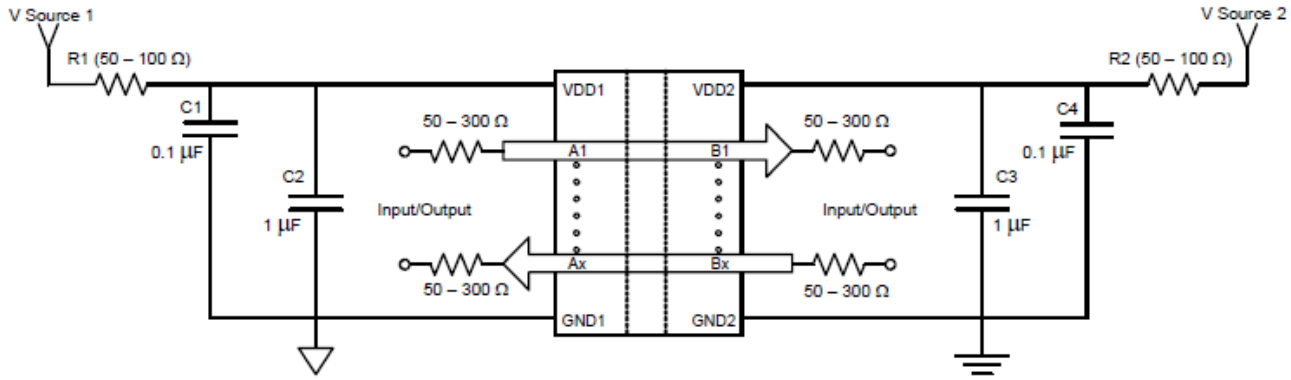


Figure 6. Recommended Bypass Components for the ILX488-3 Digital Isolator Family

2.5. Typical Performance Characteristics

The typical performance characteristics depicted in the following diagrams are for information purposes only. Refer to Tables 3, 4, and 5 for actual specification limits.

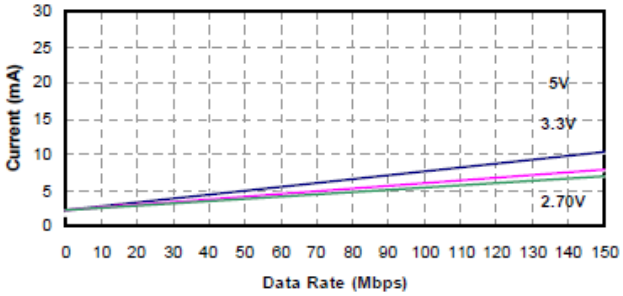


Figure 7. Si8431 Typical VDD1 Supply Current vs. Data Rate 5, 3.3, and 2.70 V Operation

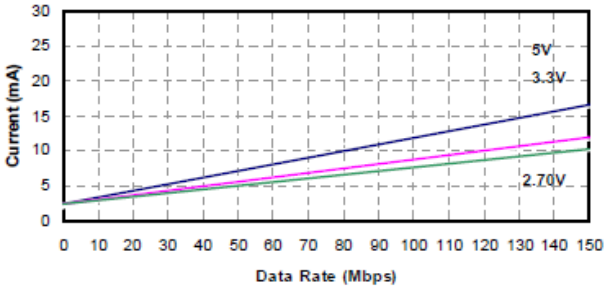


Figure 8. ILX488-3 Typical VDD2 Supply Current vs. Data Rate 5, 3.3, and 2.70 V Operation (15 pF Load)

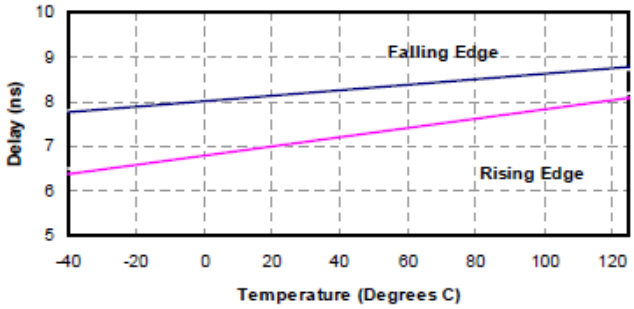


Figure 9. Propagation Delay vs. Temperature

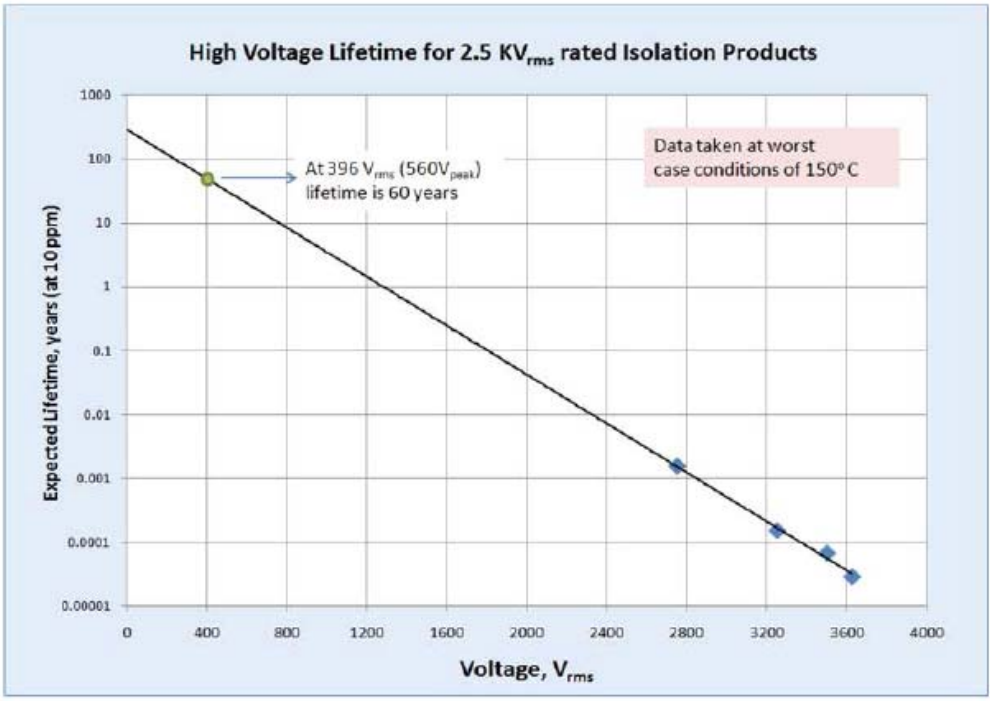


Figure 10. ILX488-3 Time-Dependent Dielectric Breakdown

3. Design Migration Guidelines

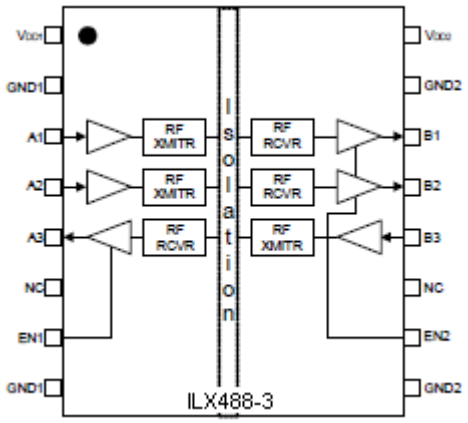
3.1. Power Supply Bypass Capacitors

When using the ILX488-3 isolators with power supplies > 4.5 V, sufficient VDD bypass capacitors must be present on both the VDD1 and VDD2 pins to ensure the VDD rise time is less than 0.5 V/µs (which is > 9 µs for a > 4.5 V supply). Although rise time is power supply dependent, > 1 µF capacitors are required on both power supply pins (VDD1, VDD2) of the isolator device.

3.2.1. Resolution

For recommendations on resolving this issue, see "2.3.1. Supply Bypass" on page 12. Additionally, refer to "5. Ordering Guide" on page 17 for current ordering information.

Package Descriptions



Name	SOIC-16 Pin#	Type	Description[1]
V_{DD1}	1	Supply	Side 1 power supply.
GND1	2	Ground	Side 1 ground.
A1	3	Digital Input	Side 1 digital input.
A2	4	Digital Input	Side 1 digital input.
A3	5	Digital I/O	Side 1 digital input or output.
NC	6	NA	No Connect.
EN1/NC[2]	7	Digital Input	Side 1 active high enable. NC on Si8430/35
GND1	8	Ground	Side 1 ground.
GND2	9	Ground	Side 2 ground.
EN2/NC[2]	10	Digital Input	Side 2 active high enable. NC on Si8435.
NC	11	NA	No Connect.
B3	12	Digital I/O	Side 2 digital input or output.
B2	13	Digital Output	Side 2 digital output.
B1	14	Digital Output	Side 2 digital output.
GND2	15	Ground	Side 2 ground.
V_{DD2}	16	Supply	Side 2 power supply.

Notes:
1. For narrow-body devices, Pin 2 and Pin 8 GND must be externally connected to respective ground. Pin 9 and Pin 15 must also be connected to external ground.
2. No Connect. These pins are not internally connected. They can be left floating, tied to VDD or tied to GND.

4. Ordering Guide

Table 14. Ordering Guide for Valid OPNs[1]

Ordering Part Number (OPN)	Number of Inputs VDD1 Side	Number of Inputs VDD2 Side	Maximum Data Rate (Mbps)	Isolation Rating	Temp Range	Package Type
ILX488-3	2	1	1	2.5 kVrms	–40 to 125 °C	NB SOIC-161

Notes:
1. All packages are RoHS-compliant.
Moisture sensitivity level is MSL2A for narrow-body SOIC-16 packages with peak reflow temperatures of 260 °C according to the JEDEC industry standard classifications and peak solder temperatures.
2. AEC-Q100 qualified.

5. Package Outline: 16-Pin Narrow Body SOIC

Figure 11 illustrates the package details for the ILX488-3 in a 16-pin narrow-body SOIC (SO-16). Table 15 lists the values for the dimensions shown in the illustration.

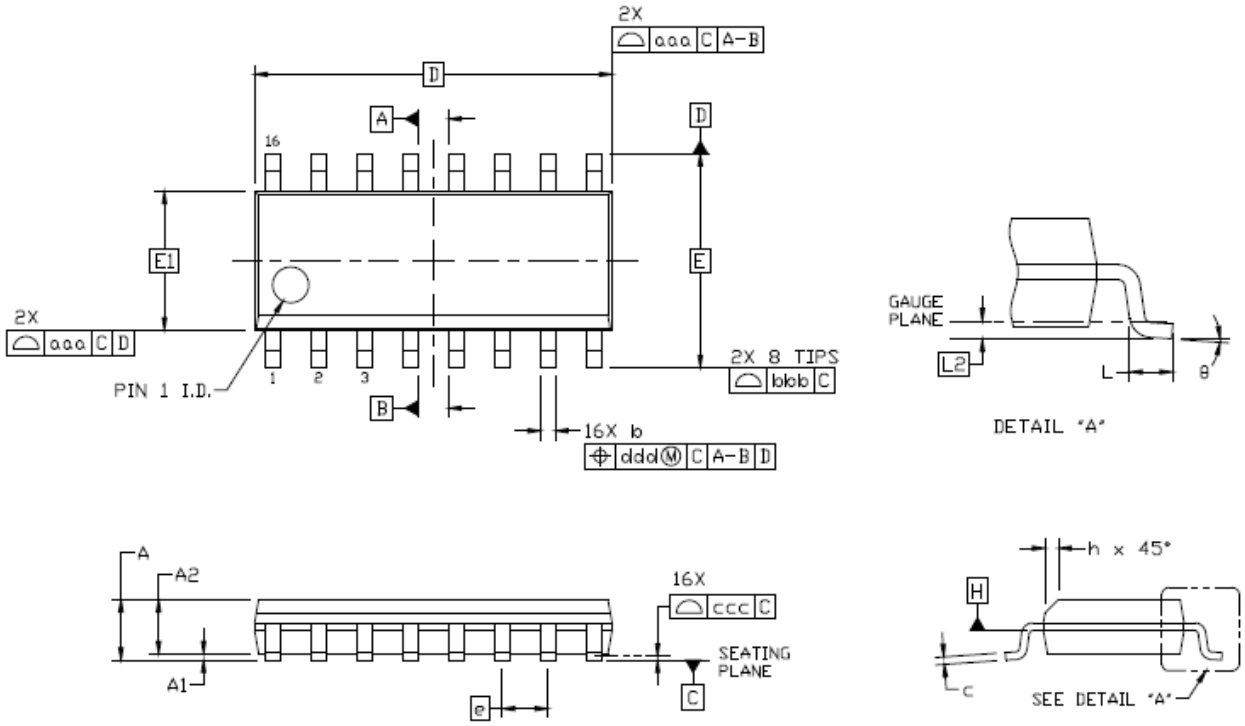


Figure 11. 16-pin Small Outline Integrated Circuit (SOIC) Package

Table 15. Package Diagram Dimensions

Dimension	Min	Max
A	—	1.75
A1	0.10	0.25
A2	1.25	—
b	0.31	0.51
c	0.17	0.25
D	9.90 BSC	
E	6.00 BSC	
E1	3.90 BSC	
e	1.27 BSC	
L	0.40	1.27
L2	0.25 BSC	

Table 15. Package Diagram Dimensions (Continued)

h	0.25	0.50
θ	0°	8°
aaa	0.10	
bbb	0.20	
ccc	0.10	
ddd	0.25	

Notes:

1. All dimensions shown are in millimeters (mm) unless otherwise noted.
2. Dimensioning and Tolerancing per ANSI Y14.5M-1994.
3. This drawing conforms to the JEDEC Solid State Outline MS-012, Variation AC.
4. Recommended card reflow profile is per the JEDEC/IPC J-STD-020 specification for Small Body Components.

6. Land Pattern: 16-Pin Narrow Body SOIC

Figure 12 illustrates the recommended land pattern details for the ILX488-3 in a 16-pin narrow-body SOIC. Table 16 lists the values for the dimensions shown in the illustration.

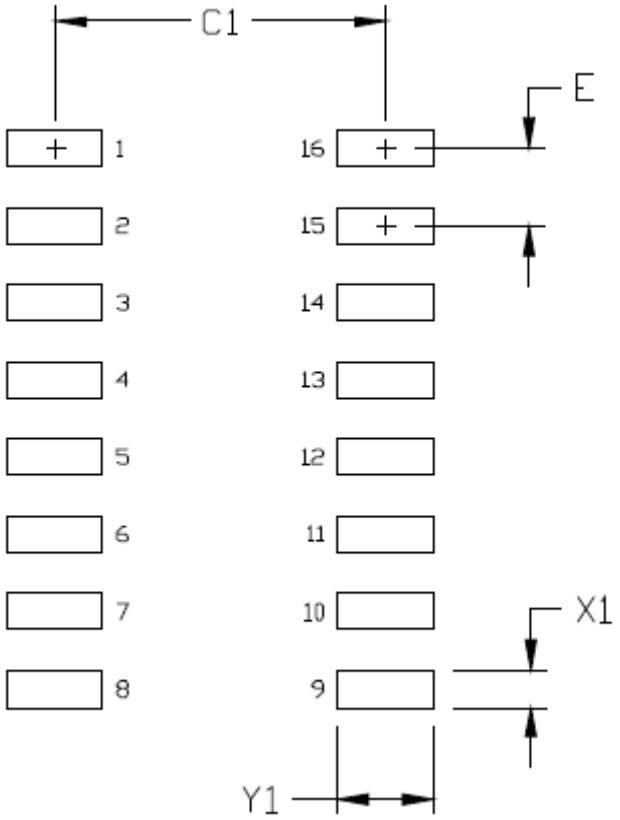


Figure 12. 16-Pin Narrow Body SOIC PCB Land Pattern

Table 16. 16-Pin Narrow Body SOIC Land Pattern Dimensions

Dimension	Feature	(mm)
C1	Pad Column Spacing	5.40
E	Pad Row Pitch	1.27
X1	Pad Width	0.60
Y1	Pad Length	1.55

Notes:

1. This Land Pattern Design is based on IPC-7351 pattern SOIC127P600X165-16N for Density Level B (Median Land Protrusion).
2. All feature sizes shown are at Maximum Material Condition (MMC) and a card fabrication tolerance of 0.05 mm is assumed.