Voltage Controlled Silicon Oscillator

IK6990

FEATURES

- **Fixed-Frequency or Voltage-Controlled Operation**
  - **Fixed-Frequency or VoltageControlled Operation with <1.5% Max Error**
  - **VCO: Two Resistors Set VCO Center**
- **Frequency Range: 488Hz to 2MHz**
- 2.25V to 5.5V Single Supply Operation
- 72µA Supply Current at 62.5kHz
- 500µs Start-Up Time
- VCO Bandwidth >300kHz at 1MHz
- CMOS Logic Output Sources/Sinks 20mA
- 50% Duty Cycle Square Wave Output
- Output Enable (Selectable Low or Hi-Z When Disabled)
- -40°C to 85°C Operating Temperature Range
- Available in Low profile SOT-23(ThinSOT) and DFN Package

APPLICATIONS

- Low Cost Precision Programmable Oscillator
- Voltage-Controlled Oscillator
- High Vibration, High Acceleration Environments
- Replacement for Fixed Crystal and Ceramic Oscillators
- Portable and Battery-Powered Equipment

DESCRIPTION

The IK6990 is a precision silicon oscillator with a programmable frequency range of 488Hz to 2MHz. It can be used as a fixed-frequency or voltage-controlled oscillator (VCO). The IK6990 can be used with the TimerBlox family of versatile silicon timing devices.

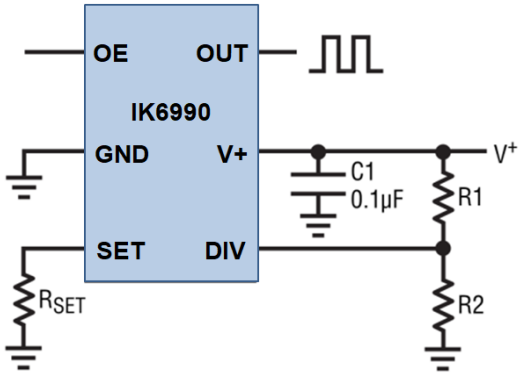
A single resistor, R_{SET} , programs the IK6990's internal master oscillator frequency. The output frequency is determined by this master oscillator and an internal frequency divider, N_{DIV}, programmable to eight settings from 1 to 128.

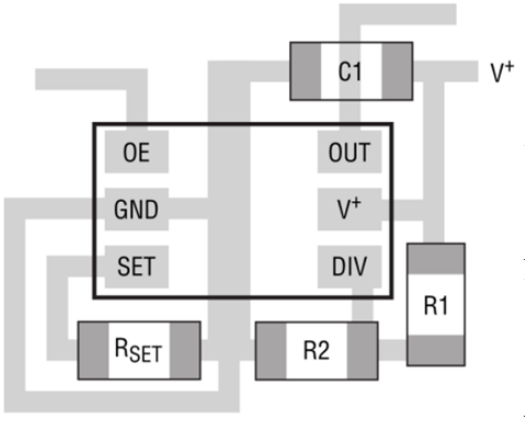
$$f_{out} = \frac{1MHz}{N_{DIV}} \times \frac{50k\Omega}{R_{SET}} \quad , N_{DIV} = 1,2,4...128$$

Optionally, a second resistor at the SET input provides linear voltage control of the output frequency and can be used for frequency modulation. A narrow or wide VCO tuning range can be configured by the appropriate selection of the two resistors.

The IK6990 includes an enable function that is synchronized with the master oscillator to ensure clean, glitch-free output pulses. The disabled output can be configured to be high impedance or forced low.

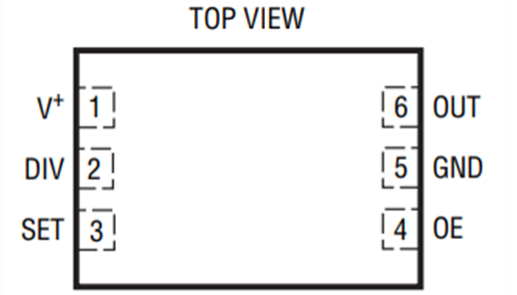
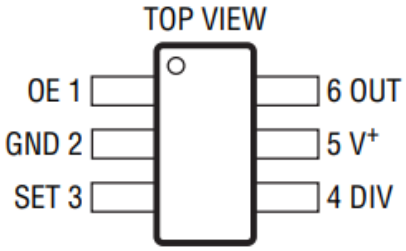
TYPICAL APPLICATION





TSOT-23 PACKAGE

ORDER INFORMATION

Device	IK6990DNT	IK6990S2T (IK6990TS2T)
Package	6-DFN	SOT-23-6 (TSOT-23-6)
Pin configuration		

ELECTRICAL CHARACTERISTICS

Graphical Symbol	Characteristic Name	Measuring mode	Nominal		Temperature, ℃	Unit
			Min	Max		
V_{OL11}	Output voltage of low level	V_{CC} = 5.5V, V_{IL} = 0V, V_{IH} = 5.5V, I_{OL} = -1mA	-	0.04	25±5; -40~85	V
V_{OL12}		V_{CC} = 5.5V, V_{IL} = 0V, V_{IH} = 5.5V, I_{OL} = -16mA	-	0.54		
V_{OL21}		V_{CC} = 3.3V, V_{IL} = 0V, V_{IH} = 3.3V, I_{OL} = -1mA	-	0.05		
V_{OL22}		V_{CC} = 3.3V, V_{IL} = 0V, V_{IH} = 3.3V, I_{OL} = -10mA	-	0.46		
V_{OL31}		V_{CC} = 2.25V, V_{IL} = 0V, V_{IH} = 2.25V, I_{OL} = -1mA	-	0.07		
V_{OL32}		V_{CC} = 2.25V, V_{IL} = 0V, V_{IH} = 2.25V, I_{OL} = -8mA	-	0.54		
V_{OH11}	Output voltage of high level	V_{CC} = 5.5V, V_{IL} = 0V, V_{IH} = 5.5V, I_{OL} = 1mA	5.45	-	25±5; -40~85	V
V_{OH12}		V_{CC} = 5.5V, V_{IL} = 0V, V_{IH} = 5.5V, I_{OL} = 16mA	4.84	-		
V_{OH21}		V_{CC} = 3.3V, V_{IL} = 0V, V_{IH} = 3.3V, I_{OL} = 1mA	3.24	-		
V_{OH22}		V_{CC} = 3.3V, V_{IL} = 0V, V_{IH} = 3.3V, I_{OL} = 10mA	2.75	-		
V_{OH31}		V_{CC} = 2.25V, V_{IL} = 0V, V_{IH} = 2.25V, I_{OL} = 1mA	2.17	-		
V_{OH32}		V_{CC} = 2.25V, V_{IL} = 0V, V_{IH} = 2.25V, I_{OL} = 8mA	1.58	-		
I_{IL}	Low level input current	V_{CC} = 5.5V, V_{IL} = 0V	-	-10.0	25±5; -40~85	nA
I_{IH}	High level input current	V_{CC} = 5.5V, V_{IH} = 5.5V	-	10.0	25±5; -40~85	nA
I_{OL}	Third state output current for OUT	V_{CC} = 5.5V, V_{IL} = 0V V_{IH}=5.5V	-	10.0	25±5	uA

ELECTRICAL CHARACTERISTICS(Continue)

Graphical Symbol	Characteristic Name	Measuring mode	Nominal		Temperature, ℃	Unit
			Min	Max		
I_{S11}	Supply current	V_{CC} =5.5V, V_{DIV} =0V, V_{IH} = 5.5V R_{LOAD} =∞ ,R_{SET} =50kΩ	-	283	25±5; -40~85	uA
I_{S12}		V_{CC} =2.25V, V_{DIV} =0V, V_{IH} = 2.25V R_{LOAD} =∞ ,R_{SET} =50kΩ	-	183		
I_{S21}		V_{CC} =5.5V, V_{DIV} =0V, V_{IH} = 5.5V R_{LOAD} =∞ ,R_{SET} =800kΩ	-	105		
I_{S22}		V_{CC} =2.25V, V_{DIV} =0V, V_{IH} = 2.25V R_{LOAD} =∞ ,R_{SET} =800kΩ	-	92		
I_{S31}		V_{CC} =5.5V, V_{DIV} =1.05V, V_{IH} = 5.5V R_{LOAD} =∞ ,R_{SET} =50kΩ	-	180		
I_{S32}		V_{CC} =2.25V,V_{DIV} =1.05V, V_{IH} = 2.25V R_{LOAD} =∞ ,R_{SET} =50kΩ	-	145		
I_{S41}		V_{CC} =5.5V, V_{DIV} =1.05V, V_{IH} = 5.5V R_{LOAD} =∞ ,R_{SET} =800kΩ	-	100		
I_{S42}		V_{CC} =2.25V, V_{DIV} =1.05V, V_{IH} = 2.25V R_{LOAD} =∞ ,R_{SET} =800kΩ	-	90		
Δf_{OUT1}	Oscillator error	V_{CC} = 5.5V, V_{IL} = V_{DIV}, V_{IH} = 5.5V	-	1.5	25±5; -40~85	%
		V_{CC} = 2.25V, V_{IL} = V_{DIV}, V_{IH} = 2.25V	-	2.2		
Δf_{OUT2}		V_{CC} = 5.5V, V_{IL} = V_{DIV}, V_{IH} = 5.5V	-	2.4		
		V_{CC} = 2.25V, V_{IL} = V_{DIV}, V_{IH} = 2.25V	-	3.2		
Δf_{OUT_V1}	Oscillator frequency dependence on supply voltage	V_{CC} = 4.5 to 5.5V V_{IL} = 0V, V_{IH} = 5.5V	-	0.95	25±5; -40~85	%/V
Δf_{OUT_V1}		V_{CC} = 2.25 to 4.5V V_{IL} = 0V, V_{IH} = 2.25V	-	0.16		
f_{DC1}	Off duty factor	V_{CC} = 5.5V, V_{IL} = 0V V_{IH} = 5.5V	47	53	25±5; -40~85	%
		V_{CC} = 2.25V, V_{IL} = 0V V_{IH} = 2.25V				
f_{DC2}		V_{CC} = 5.5V, V_{IL} = 2.57V V_{IH} = 5.5V	48	52	25±5; -40~85	
		V_{CC} = 2.25V, V_{IL} = 1.05V V_{IH} = 2.25V				
V_{SET}	SET pad voltage	V_{CC} = 5.5V, V_{IH} = 5.5V	0.97	1.03	25±5; -40~85	V
		V_{CC} = 2.25V, V_{IH} = 2.25V				

Note
1) <<Minus>> sign before current norm in tables points on current direction only (drain current). Current value is absolute value of readings of current meter.
2) In the table are the parameters for the chip in package.

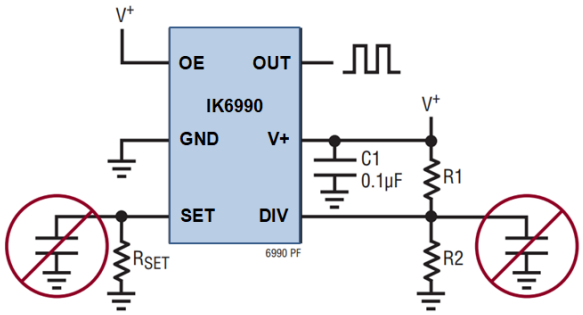
PIN FUNCTIONS

V+ : Supply Voltage (2.25V to 5.5V). This supply must be kept free from noise and ripple. It should be bypassed directly to the GND pin with a 0.1µF capacitor.

DIV : Programmable Divider and Hi-Z Mode Input. A V+ referenced A/D converter monitors the DIV pin voltage (V_{DIV}) to determine a 4-bit result (DIVCODE).
V_{DIV} may be generated by a resistor divider between V+ and GND. Use 1% resistors to ensure an accurate result. The DIV pin and resistors should be shielded from the OUT pin or any other traces that have fast edges. Limit the capacitance on the DIV pin to less than 100pF so that V_{DIV} settles quickly. The MSB of DIVCODE (Hi-Z) determines the behavior of the output when OE is driven low. If Hi-Z = 0 the output is pulled low when disabled. If Hi-Z = 1 the output is placed in a high impedance condition when disabled.

SET : Frequency-Setting Input. The voltage on the SET pin (V_{SET}) is regulated to 1V above GND. The amount of current sourced from the SET pin (I_{SET}) programs the master oscillator frequency. The I_{SET} current range is 1.25µA to 40µA. The output oscillation will stop if I_{SET} drops below approximately 500nA. A resistor connected between SET and GND is the most accurate way to set the frequency. For best performance, use a precision metal or thin film resistor of 0.5% or better tolerance and 50ppm/°C or better temperature coefficient. For lower accuracy applications an inexpensive 1% thick film resistor may be used.

Limit the capacitance on the SET pin to less than 10pF to minimize jitter and ensure stability. Capacitance less than 10pF maintains the stability of the feedback circuit regulating the V_{SET} voltage.



OE : Output Enable. Drive high to enable the output driver. Driving OE low disables the output asynchronously, so that the output is immediately forced low (Hi-Z = 0) or floated (Hi-Z = 1). When enabled, the output may temporarily remain low to synchronize with the internal oscillator in order to eliminate pulse slivers.

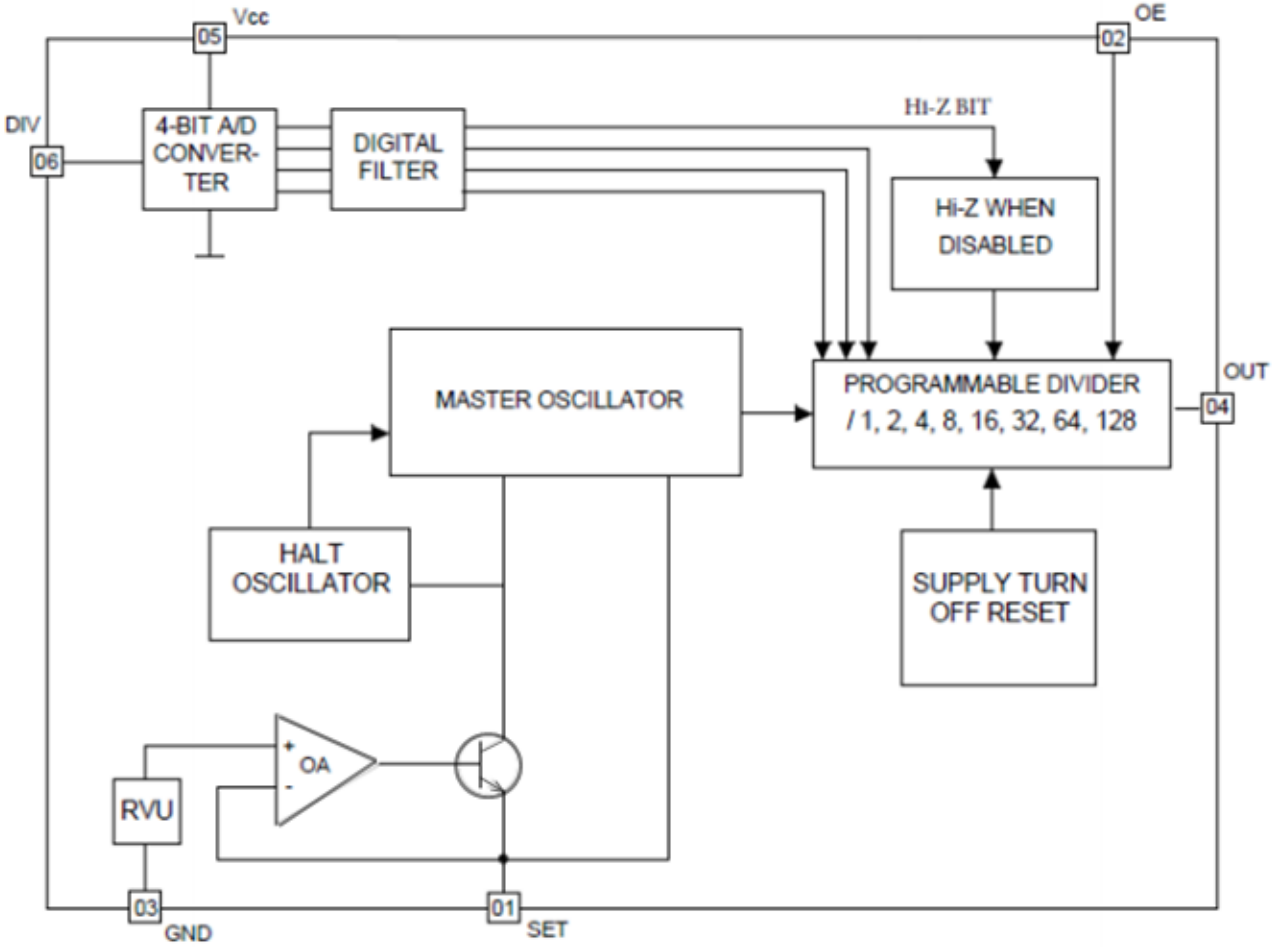
GND : Ground. Tie to a low inductance ground plane for best performance.

OUT : Oscillator Output. The OUT pin swings from GND to V+ with an output resistance of approximately 30Ω . When driving an LED or other low-impedance load a series output resistor should be used to limit source/sink current to 20mA.

CONTACT PAD FUNCTION AND NUMBERATION

Chip contact pad number	Graphical symbol	Function
01	SET	Frequency tunning
02	OE	Output enable input
03	GND	Common
04	OUT	Frequency generation output
05	V_{CC}	Supply
06	DIV	Frequency divider input

BLOCK DIAGRAM



OPERATION

The IK6990 is built around a master oscillator with a 1MHz maximum frequency. The oscillator is controlled by the SET pin current (I_{SET}) and voltage (V_{SET}), with a 1MHz • 50k conversion factor that is accurate to ±0.8% under typical conditions.

$$f_{MASTER} = \frac{1}{t_{MASTER}} = 1MHz * 50k * \frac{I_{SET}}{V_{SET}}$$

A feedback loop maintains V_{SET} at 1V ±30mV, leaving I_{SET} as the primary means of controlling the output frequency. The simplest way to generate I_{SET} is to connect a resistor (R_{SET}) between SET and GND, such that $I_{SET} = V_{SET} / R_{SET}$. The master oscillator equation reduces to:

$$f_{MASTER} = \frac{1}{t_{MASTER}} = \frac{1MHz * 50k}{R_{SET}}$$

From this equation it is clear that V_{SET} drift will not affect the output frequency when using a single program resistor (R_{SET}). Error sources are limited to R_{SET} tolerance and the inherent frequency accuracy Δf_{OUT} of the IK6990. R_{SET} values between 50k and 800k (equivalent to I_{SET} between 1.25µA and 20µA) produce the best results, although R_{SET} may be reduced to 25k (I_{SET} = 40µA) with reduced accuracy. The IK6990 includes a programmable frequency divider which can further divide the frequency by 1, 2, 4, 8, 16, 32, 64 or 128 before driving the OUT pin. The divider ratio N_{DIV} is set by a resistor divider attached to the DIV pin.

$$f_{OUT} = \frac{1}{t_{OUT}} = \frac{1MHz * 50k}{N_{DIV}} * \frac{I_{SET}}{V_{SET}}$$

With R_{SET} in place of V_{SET} / I_{SET} the equation reduces to:

$$f_{OUT} = \frac{1}{t_{OUT}} = \frac{1MHz * 50k}{N_{DIV} * R_{SET}}$$

DIVCODE

The DIV pin connects to an internal, V+ referenced 4-bit A/D converter that monitors the DIV pin voltage (V_{DIV}) to determine the DIVCODE value. DIVCODE programs two settings on the IK6990:

1. DIVCODE determines the output frequency divider setting, N_{DIV}.

2. DIVCODE determines the state of the output when disabled, via the Hi-Z bit.

V_{DIV} may be generated by a resistor divider between V+ and GND as shown in Figure 1.

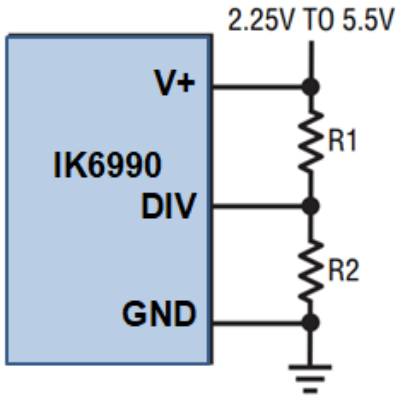


Figure 1. Simple Technique for Setting DIVCODE

Table 1. DIVCODE Programming

DIVCODE	Hi-Z	N_{DIV}	Recommended f_{OUT}	R_1(k)	R_2(k)	V_{DIV}/V_{CC}
0	0	1	62.5kHz to 1MHz	Open	Short	≤ 0.03125±0.015%
1	0	2	31.25kHz to 500kHz	976	102	0.09375±0.015%
2	0	4	15.63kHz to 250kHz	976	182	0.15625±0.015%
3	0	8	7.813kHz to 125kHz	1000	280	0.21878±0.015%
4	0	16	3.906kHz to 62.5kHz	1000	392	0.28125±0.015%
5	0	32	1.953kHz to 31.25kHz	1000	523	0.34375±0.015%
6	0	64	976.6Hz to 15.63kHz	1000	681	0.40625±0.015%
7	0	128	488.3Hz to 7.813kHz	1000	887	0.46875±0.015%
8	1	128	488.3Hz to 7.813kHz	887	1000	0.53125±0.015%
9	1	64	976.6Hz to 15.63kHz	681	1000	0.59375±0.015%
10	1	32	1.953kHz to 31.25kHz	523	1000	0.65625±0.015%
11	1	16	3.906kHz to 62.5kHz	392	1000	0.71875±0.015%
12	1	8	7.813kHz to 125kHz	280	1000	0.78125±0.015%
13	1	4	15.63kHz to 250kHz	182	976	0.84375±0.015%
14	1	2	31.25kHz to 500kHz	102	976	0.90629±0.015%
15	1	1	62.5kHz to 1MHz	Short	Open	≥ 0.96875±0.015%

Table 1 offers recommended 1% resistor values that accurately produce the correct voltage division as well as the corresponding N_{DIV} and Hi-Z values for the recommended resistor pairs. Other values may be used as long as:

1. The $V_{DIV}/V+$ ratio is accurate to ±1.5% (including resistor tolerances and temperature effects)

2. The driving impedance ($R_1||R_2$) does not exceed 500kΩ .

If the voltage is generated by other means (i.e. the output of a DAC) it must track the V+ supply voltage. The last column in Table 1 shows the ideal ratio of V_{DIV} to the supply voltage,

which can also be calculated as:

$$\frac{V_{DIV}}{V_{CC}} = \frac{DIVCODE + 0.5}{16} \pm 1.5\%$$

For example, if the supply is 3.3V and the desired DIVCODE is 4, V_{DIV} = 0.281 • 3.3V = 928mV ± 50mV.

Figure 2 illustrates the information in Table 1, showing that N_{DIV} is symmetric around the DIVCODE midpoint. On start-up, the DIV pin A/D converter must determine the correct DIVCODE before the output is enabled. If V_{DIV} is not stable, it will increase the start-up time as the converter waits for a stable result. Therefore, capacitance on the DIV pin should be minimized so it will settle quickly. Less than 100pF will not affect performance.

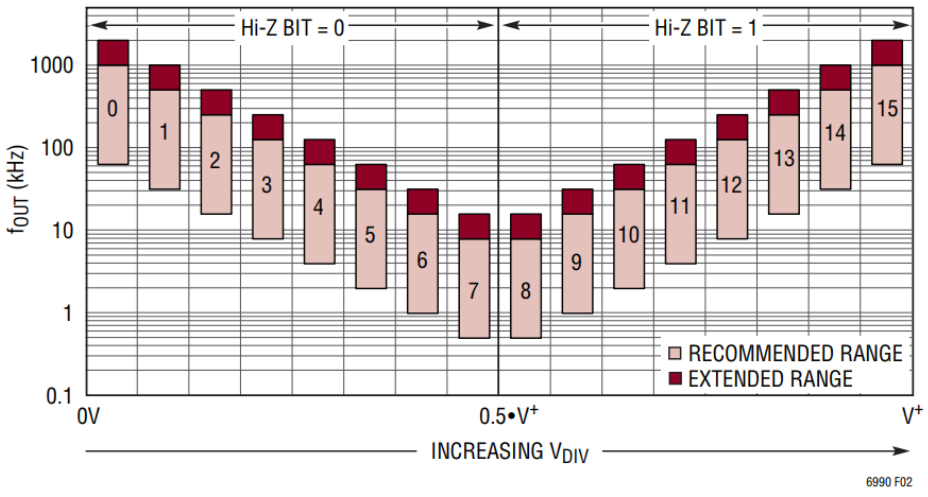


Figure 2. Frequency Range and Hi-Z Bit vs DIVCODE

Output Enable

The OE pin controls the state of the IK6990's output as seen on the OUT pin. Pulling the OE pin high enables the oscillator output. Pulling it low disables the output. When the output is disabled, it is either held low or placed in a high impedance state as dictated by the Hi-Z bit value (determined by the DIVCODE as described earlier). Table 2 summarizes the output control states.

Table 2. Output states

OE Pin	Hi-Z	OUT
1	X	Enabled, Output is Active
0	1	Disabled, Output is Hi-Z
0	0	Disabled, Output is Held Low

Figure 3 illustrates the timing for the OE function when Hi-Z = 0. When OE is low, the output is disabled and OUT is held low. Bringing OE high enables the output after a delay, t_{ENABLE}, which synchronizes the enable to eliminate sliver pulses and guarantee the correct width for the first pulse. If N_{DIV} = 1 or 2 this delay will be no longer than the output period, t_{OUT}. If N_{DIV} > 2 the delay is limited to twice the internal master oscillator period (or $2 \cdot t_{MASTER}$). Forcing OE low will bring OUT low after a propagation delay, t_{PD}. If the output is high when OE falls, the output PD pulse will be truncated.

As shown in Figure 4, setting Hi-Z = 1 places the output in a high-impedance state when OE = 0. This feature allows for "wired-OR" connections of multiple devices. Driving OE high enables the output. The output will usually be forced low during this time, although it is possible for OUT to transition directly from high-impedance to a high output, depending on the timing of the OE transition relative to the internal oscillator. Once high, the first output pulse will have the correct width (unless truncated by bringing OE low again).

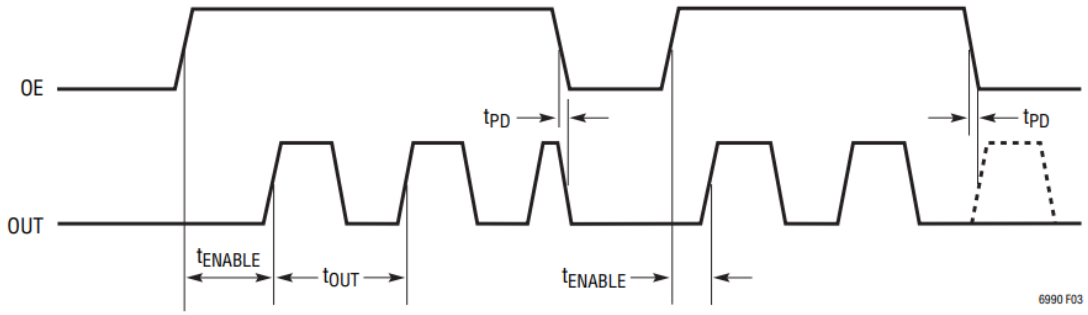


Figure 3. OE Timing Diagram (Hi-Z = 0)

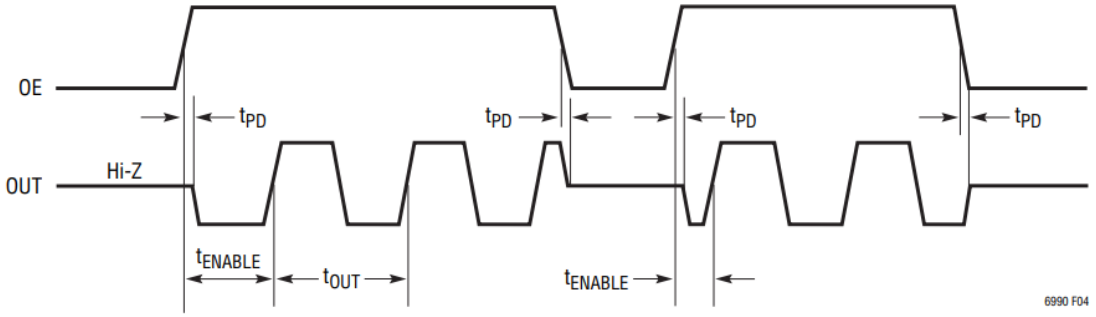


Figure 4. OE Timing Diagram (Hi-Z = 1)

Changing DIVCODE After Start-Up

Following start-up, the A/D converter will continue monitoring V_{DIV} for changes. Changes to DIVCODE will be recognized slowly, as the IK6990 places a priority on eliminating any "wandering" in the DIVCODE. The typical delay depends on the difference between the old and new DIVCODE settings and is proportional to the master oscillator period.

$$t_{DIVCODE} = 16 \bullet (\Delta DIVCODE + 6) \bullet t_{MASTER}$$

A change in DIVCODE will not be recognized until it is stable, and will not pass through intermediate codes. A digital filter is used to guarantee the DIVCODE has settled to a new value before making changes to the output. Then the output will make a clean (glitchless) transition to the new divider setting.

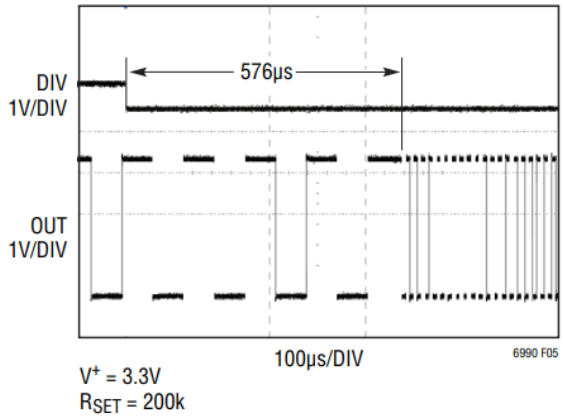


Figure 5. DIVCODE Change from 5 to 2

Start-Up Time

When power is first applied to the IK6990 the power-on reset (POR) circuit will initiate the start-up time, t_{START}. The OUT pin is floated (high-impedance) during this time. The typical value for t_{START} ranges
from 0.5ms to 8ms depending on the master oscillator frequency (independent of N_{DIV}):

$$t_{START(TYP)} = 500 \bullet t_{MASTER}$$

The start-up time may be longer if the supply or DIV pin voltages are not stable. For this reason, it is recommended to minimize the capacitance on the DIV pin so it will properly track V+.

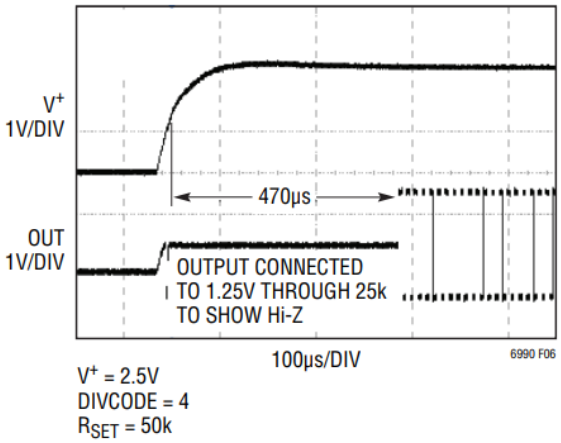
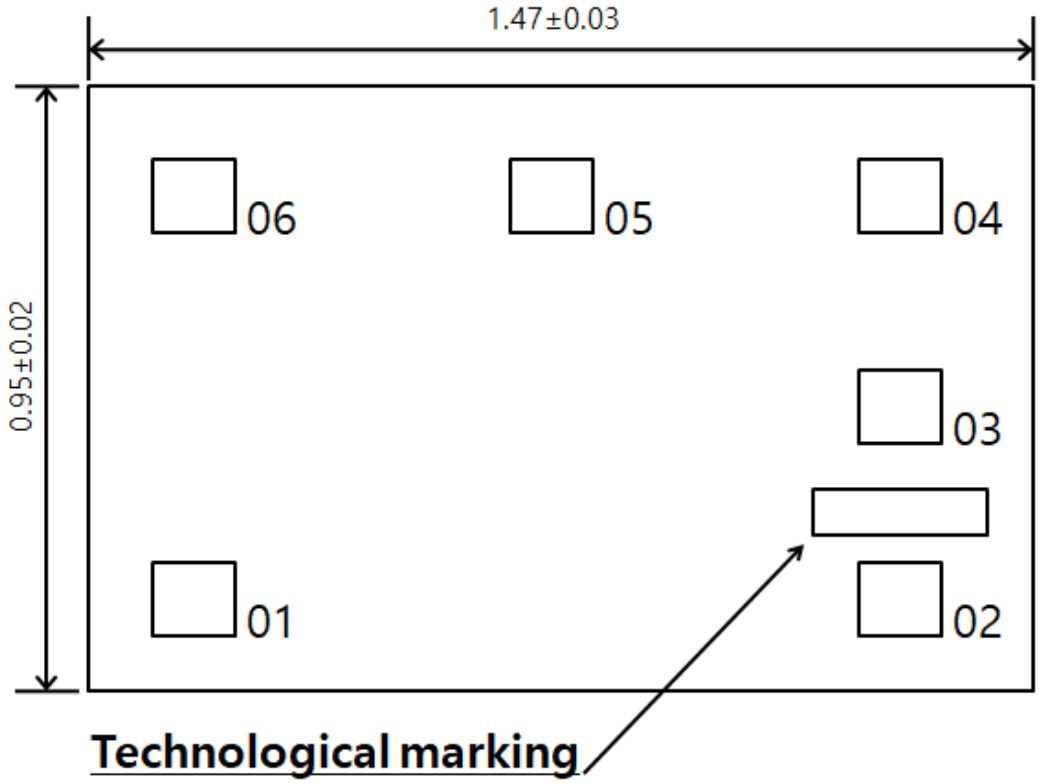


Figure 6. Typical Start-Up

CHIP OVERALL DIMENSION DRAFT



«12 6990» is Technological marking on chip with coordinates in mm :
left lower corner x =1.3088 , y = 0.2924.
Chip thickness - 0,46 ± 0,02 mm.
Contact pads coordinates are indication in table

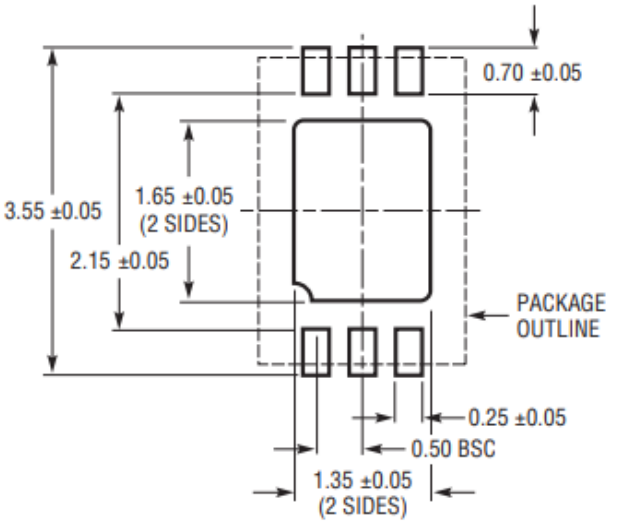
COORDINATES OF CONTACT PADS

Number of Contact Pad	Coordinates(Left Bottom Corner) , mm		Size of Contact Pad, mm
	X	Y	
01	0.115	0.163	0.090x0.090
02	1.265	0.163	
03	1.265	0.340	
04	1.270	0.706	
05	0.765	0.707	
06	0.115	0.698	
Note - Coordinates and size of the contact pads are provided as per the layer « Passivation».			

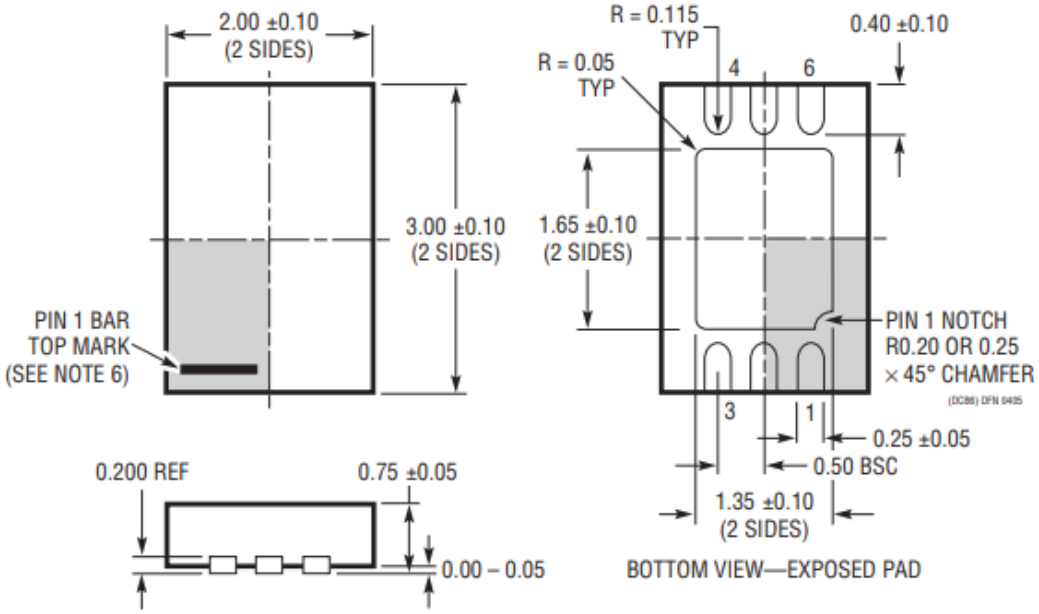
Metal Composition of the Planar Side		Metal Thickness on the planar Side, um
Metallization 1	Ti	0.020 ± 0.002
	AlCu	0.60 ± 0.06
	Ti	0.020 ± 0.002
	TiN	0.050 ± 0.005
Metallization 2	Ti	0.020 ± 0.002
	AlCu	0.80 ± 0.08
	TiN	0.050 ± 0.005

PACKAGE DESCRIPTION

6-Lead Plastic DFN(2mm * 3mm)



RECOMMENDED SOLDER PAD PITCH AND DIMENSIONS

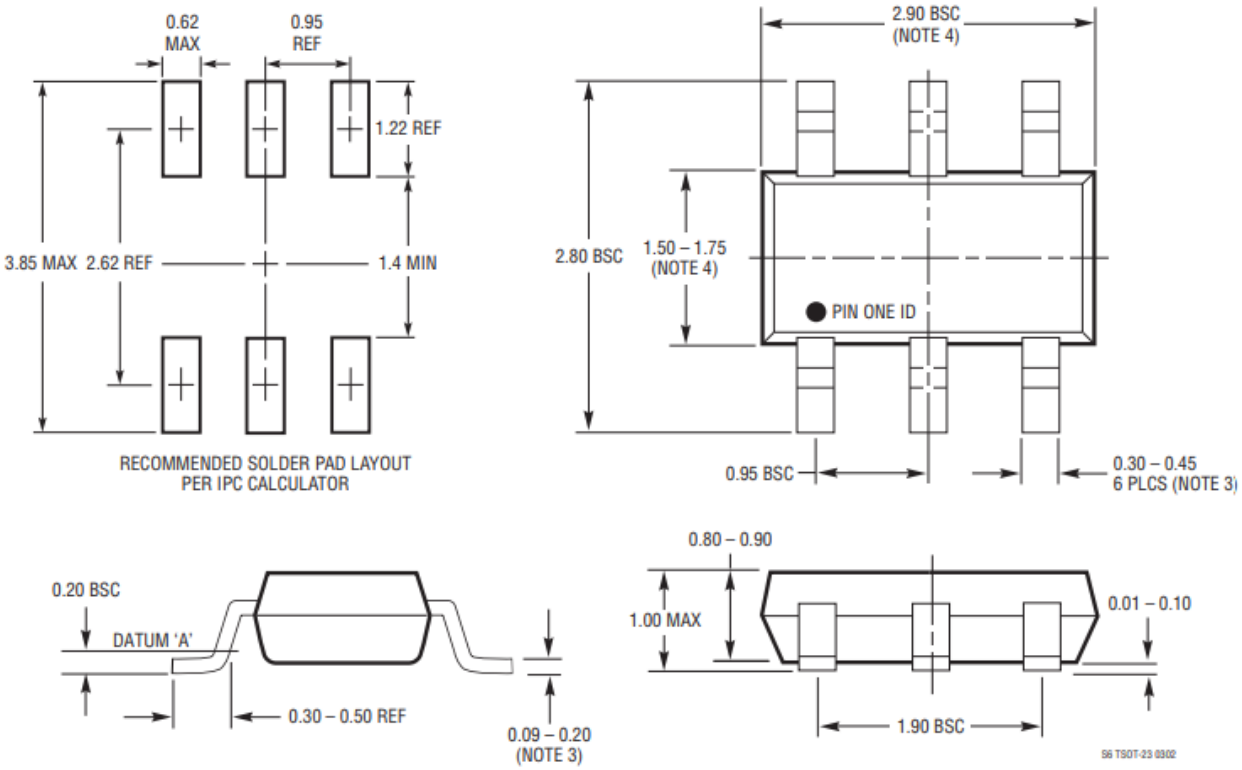


BOTTOM VIEW—EXPOSED PAD

NOTE:
1. DRAWING TO BE MADE A JEDEC PACKAGE OUTLINE M0-229 VARIATION OF (TBD)
2. DRAWING NOT TO SCALE
3. ALL DIMENSIONS ARE IN MILLIMETERS
4. DIMENSIONS OF EXPOSED PAD ON BOTTOM OF PACKAGE DO NOT INCLUDE MOLD FLASH. MOLD FLASH, IF PRESENT, SHALL NOT EXCEED 0.15mm ON ANY SIDE
5. EXPOSED PAD SHALL BE SOLDER PLATED
6. SHADED AREA IS ONLY A REFERENCE FOR PIN 1 LOCATION ON THE TOP AND BOTTOM OF PACKAGE

PACKAGE DESCRIPTION

6-Lead Plastic TSOT-23



NOTE:
1. DIMENSIONS ARE IN MILLIMETERS
2. DRAWING NOT TO SCALE
3. DIMENSIONS ARE INCLUSIVE OF PLATING
4. DIMENSIONS ARE EXCLUSIVE OF MOLD FLASH AND METAL BURR
5. MOLD FLASH SHALL NOT EXCEED 0.254mm
6. JEDEC PACKAGE REFERENCE IS MO-193